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THE ULTIMATE SOLID-STATE MEMORY?

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General Manager: J. Dhas
Advertising: B.M. Mehta
Production: C.N. Mithagari

Address:
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Bombay - 400 007 INDIA
Telex: (011) 76661 ELEK IN

Overseas editions

Elektor Electronics
Standfast House
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High Street, Barnet
Herts EN5 5XE U.K.
Editor: Len Seymour

Publitron Publicacoes Tecnicas Ltda
Av Ipiranga 1100, 9° andar
CEP 01040 Sao Paulo — Brazil
Editor: Juliano Barsali

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Route Nationale; Le Seau; B.P. 53
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Box 63
182 11 Danderyd — Sweden
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Printed At:
Trupti Offset
Bombay - 400 013
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Volume-5 Number-4
April 1987

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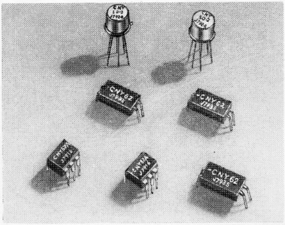
PHILIPS

PROFESSIONAL OPTOCOUPLERS FROM PHILIPS



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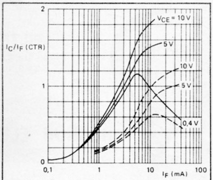

Fig.1 Current transfer rati· versus forward current.
—— Piece with a high I_C/I_F (CTR)
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type	current transfer ratio τ_{min} (see Fig. 1)			isolation voltage d.c.	photo-diode		photo-transistor		switching times V_{CC} = 5 V; $I_{C\ on}$ = 2 mA				case
									t_{on} µs		t_{off} µs		
	V_{CE} = 0,4 V I_F = 10 mA	V_{CE} = 1 V I_F = 1 mA	V_{CE} = 10 V I_F = 10 mA	kV	I_F mA	$V_{R\ max}$ V	V_{CEmax} V	$P_{tot\ max}$ mW	R_L = 2 kΩ	R_L = 100 Ω	R_L = 2 kΩ	R_L = 100 Ω	
CNX35	0,4	-	-	4,4	100	5	30	200	-	3	-	3	SOT-90B
CNX36*	0,8	-	-	4,4	100	5	30	200	-	3	-	3	SOT-90B
CNX38*	-	-	0,7	4,4	100	5	80	200	-	5	-	5	SOT-90B
CNX39	0,6	-	-	4,4	100	5	30	200	-	3	-	3	SOT-90B
CNX44	0,3	-	-	1,0	100	3	50	300	-	5	-	5	SOT-104C
CNX48*	-	5,0	-	4,4	100	5	30	200	-	5	-	30	SOT-90B
CNX62*	0,4	-	-	5,3	100	5	50	200	-	3	-	3	SOT-174
CNX72*	0,4	-	-	5,3	100	5	30	200	-	26	-	2,5	SOT-90B
CNX82*	0,4	-	-	5,3	100	5	50	200	-	3	-	3	SOT-90B
CNX91	-	-	-	0,8	100	7	50	230	-	5	-	5	SOT-18F
CNX92	-	-	-	0,8	100	7	50	230	-	-	-	-	SOT-18F
CNY50-1	0,25	-	-	1,0	100	3	50	150	20	-	70	-	SOT-104B
CNY50-2	4,0	-	-	1,0	100	5	50	150	20	-	70	-	SOT-104B
CNY57*	0,2	-	-	4,4	100	3	30	200	-	3	-	3	SOT-90B
CNY57A*	0,4	-	-	4,4	100	3	30	200	-	5	-	5	SOT-90B
MCT2*	-	-	0,2	4,4	60	3	30	200	5	-	30	-	SOT-90B
MCT26*	-	-	0,06	4,4	60	3	30	250	-	2	-	2	SOT-90B
4N25*	-	-	0,2	2,5	80	3	30	250	5	-	30	-	SOT-90B
4N25A*	-	-	0,2	2,5	80	3	30	250	5	-	30	-	SOT-90B
4N26*	-	-	0,2	1,5	80	3	30	250	5	-	30	-	SOT-90B
4N27*	-	-	0,1	1,5	80	3	30	250	5	-	30	-	SOT-90B
4N28*	-	-	0,1	0,5	80	3	30	250	5	-	30	-	SOT-90B
H11A1*	-	-	0,5	1,5	60	3	30	250	-	2	-	2	SOT-90B
H11A2*	-	-	0,2	0,950	60	3	30	250	-	2	-	2	SOT-90B
H11A3*	-	-	0,2	1,5	60	3	30	250	-	2	-	2	SOT-90B
H11A4*	-	-	0,1	0,950	60	3	30	250	-	2	-	2	SOT-90B

* These types are available with UL and VDE approval.

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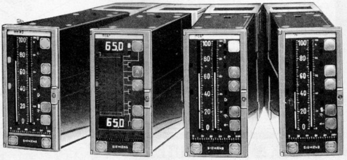

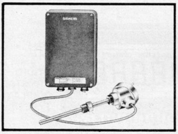

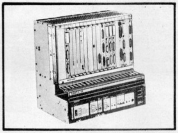

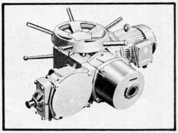

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DESIGN ABSTRACTS

The contents of this column are based on information obtained from manufacturers in the electronics industry, or their representatives, and do not imply practical experience by *Elektor Electronics* or its consultants.

PASSIVE INFRA-RED DETECTOR TYPE PID-11

The Siemens Type PID-11 infra-red detector is manufactured from heat sensitive polyvinyl-edendifluoride—PVDF—with all necessary optical and electronic elements on board.

Passive infra-red detectors are particularly suitable for observing heat emanating from mammals and converting this into an electrical signal—see Fig. 1. They are normally used for the detection of movement (which gives rise to temperature differences) and are thus ideal sensors in intruder alarms.

Although PVDF—which has only been commercially available since the 1970s—has not such a wide range of operating temperatures as other types of material used in heat sensors, such as lithium tantalum oxide, it is much cheaper and easier to manufacture. Moreover, because of the thinner membranes used, it has a much shorter response time. Figure 2 shows a Type PID-11 detector removed from its housing.

Construction

The detector consists essentially of the following elements: venetian blind; infra-red window; parabolic reflector; sensor element; amplifier circuits; and case. The venetian blind prevents random light falling onto the window and, together with the reflector, determines the pick-up pattern—see Fig. 3. The infra-red window behind the blind protects the detector from air currents and prevents soiling of the sensor element. The reflector bundles the incoming infra-red radiation. The sensor element is located at the focus of the reflector. The amplifier board, manufactured in surface-mount technology, is connected to the back of the sensor.

The case is made of conductive plastic and serves also as an effective electrical screen. Its dimensions make it possible for the detector to be installed unobtrusively—see Fig. 4.

To compensate for variations in ambient temperature, the detector contains a second sensor which is not in the path of the incoming IR beam. Only the difference in signal levels between the two sensors is fed to the amplifier.

1

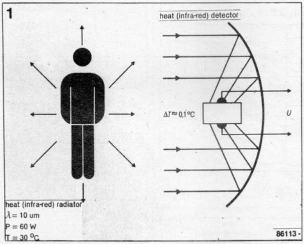

Fig. 1. Schematic representation of intruder detection with a passive infra-red device.

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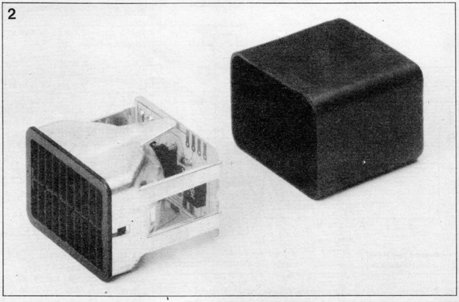

Fig. 2. Siemens passive infra-red detector Type PID-11 removed from its case.

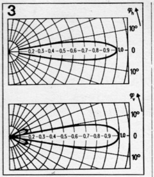

Fig. 3. Radiation pattern of the PID-11.

The circuit of the amplifier, shown in Fig. 5, is based on three inverters connected as linear amplifiers, the first one of which also serves as an impedance inverter.

The two diodes, T_1 and T_2, limit against too high inputs and also serve as high-impedance leakage resistors.

Networks R_3-C_4 and R_4-C_5 suppress low or high frequency impulse noise respectively.

A fourth inverter produces a reference voltage of

$U_{ref} = [U_b - 0.6]/2$ volts

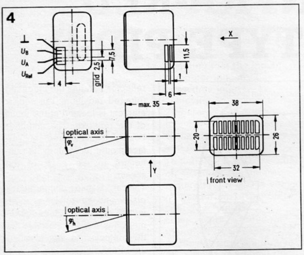

Fig. 4. Dimensions and pinout of the PID-11.

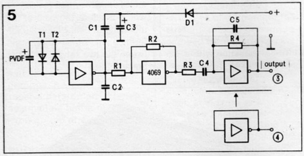

Fig. 5. Circuit diagram of the PID-11.

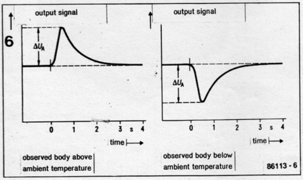

Fig. 6. Output voltage vs time characteristic when a warm or cold body is suddenly brought into the capture range of the detector.

at output 4.

Figure 6 shows the output voltage vs time characteristic during a sudden change in incoming IR radiation.

Application tips

Apart from its use in intruder alarms, the PID-11 will also be found suitable for switching on lights, water heaters, electric hand driers, and door openers. It may also be used as a counter or production monitor. The sensor is particularly sensitive to objects moving within the capture area of the detector at right angles to the optical axis. Overloading of the input by direct sunlight or other heat sources should be avoided. Very high room temperatures reduce the sensitivity of the device.

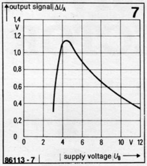

Fig. 7. Output signal vs supply voltage characteristic.

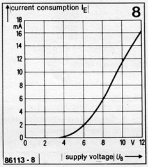

Fig. 8. Current consumption vs supply voltage.

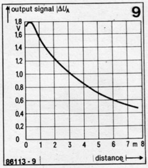

Fig. 9. Output signal vs distance of observed body within the capture range of the detector; supply voltage = 4.5 V and room temperature = 22 °C.

The main technical data are given in Table 1. A supply voltage of between 4 and 5 volts seems to be the optimum (see also Fig. 7 and Fig. 8).

The capture range of the detector depends to a large extent on the size of the object and on the difference between object and ambient temperatures—see also Fig. 9.

Table 2 shows the immunity to some light sources, and is therefore particularly useful for domestic applications.

Spurious output signals may occur just after switch-on during the heating up period.

Although the PID-11 is splash-proof, its use in the open is not recommended.

The recommended range of operating temperatures is −20 °C to +70 °C.

Some suggested circuits

In the suggested circuits in Fig. 10 and Fig. 11, the PID-11 is connected to a window comparator serving as signal detector, a timing element, and a drive circuit for the relevant application.

Fig. 10 shows a general purpose circuit, in which the window comparator is formed by OP_1 and OP_2. The reference voltage, U_{ref}, at pin 4 of the PID-11 determines the centre of the window. The upper window limit, U_1, is given by

$$U_1 = U_{ref}(R_1/R_2)$$

while the lower window limit, U_2, is given by

$$U_2 = U_{ref}[R_3/(R_3 + R_4)]$$

If the output voltage, U_a, at pin 3 of the PID-11 exceeds either of these limits, the open-collector outputs of the two opamps will be about 0.5 V, which will trigger monostable CP_3. Relay K_1 is then energized for the duration of the mono time, which is determined by C_1, R_6, and R_7. Potentiometer R_7 allows the period to be set anywhere be-

Table 1 **Technical data**

Supply voltage, Ub	4.5 V (4-12 V)
Output signal, UA (at Ub = 4.5 V)	1.1 V
Lens area	300 × 400 mm
Current consumption, IE (Ub = 4.5 V)	0.4 mA
Output impedance (CMOS) (Ub = 4.5 V)	2.2 k
Capture range (see also Fig. 9)	7 m
Response time	500 ms

Table 2 **Immunity to unwanted light**

	Maximum illumination	
	from above ϕv≧30°	from the side ϕh≧30°
Incandescent light	<800 lux	<3 000 lux
Sunlight	<10 000 lux	<20 000 lux
Fluorescent light	no effect	no effect

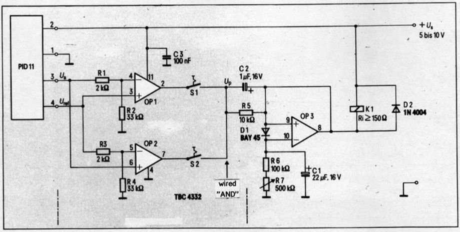

Fig. 10. General purpose application of the PID-11 with relay output.

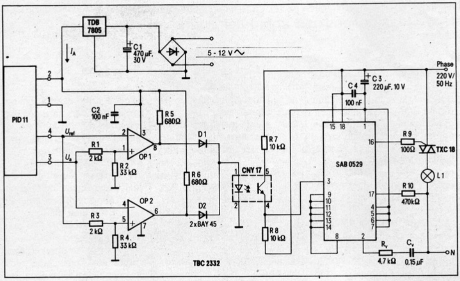

Fig. 11. Automatic staircase lighting control based on the PID-11.

tween 3 and 15 seconds.

The upper and lower limits of the window discriminator can be inactivated by S_1 or S_2 respectively: the circuit then reacts then only to a negative or positive voltage change—see Fig. 6. If, for instance, S_1 is open and S_2 closed, the relay will only be energized if a person who has been within the capture range of the detector leaves the area.

The circuit in Fig. 11 is intended for automatic operation of staircase lighting. Compared with that in Fig. 10, the window discriminator here is inverted. Lighting timer SAB0529 is triggered via an opto-coupler to ensure that the PID-11 is electrically isolated from the mains supply. The timer is set for 63 s. The power supply for the PID-11 may be formed by a bell transformer: current consumption is of the order of 10 mA.

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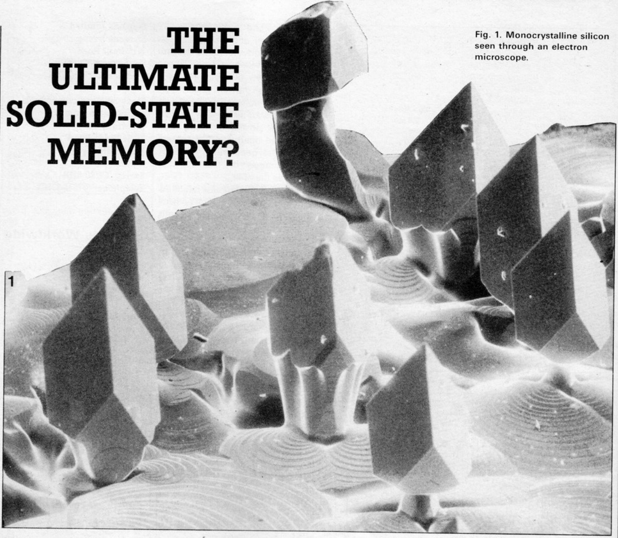


Fig. 1. Monocrystalline silicon seen through an electron microscope.

Although the super memories of the future will be predominantly photonic ones, a number of manufacturers are developing massive semiconductor memories for use in the intervening years. Many realize that they cannot make money in the memory market, but need the technology to gain experience for their telecommunications and computer businesses.

Most of the manufacturers working on the development of very large semiconductor memories have a 1Mbit DRAM (dynamic random access memory) or EPROM (erasable programmable read-only memory) in production; the remainder are poised to start production in the next few months. A number of them are also already working on the development of a 4 Mbit DRAM (for instance, the General Electric-Toshiba-Siemens-Philips conglomerate).
These devices require a state-of-the-art capability, high development and production investment, and a vast market (estimated at close to £1000 million during the economic production life, i.e., until photonic devices become available).
Most manufacturers, particularly those outside Japan, realize that they cannot make enough money in the memory market to recoup their huge investment costs. They need the technology, however, to gain experience for their telecommunications and/or computer businesses. The Japanese, unlike the Europeans and Americans, believe in a strongly growing market and rising market values.
As already stated, the investment costs associated with these super memories are so high that most manufacturers will not succeed in recovering them from the sale of the devices alone, particularly in view of the prevailing low prices on the depressed component market. It is a maxim that component prices drop by up to 90% during the first 2-3 years of the device's life. One beneficial factor is, however, that because of the high investment costs there are only a handful of competitors worldwide.
To reduce the risks, a number of manufacturers have decided on a joint venture, for instance, Siemens and Philips have jointly undertaken the development of a 4 Mbit DRAM (with the aid of the German Ministry of Research and Technology and the Dutch Ministry of Economic Affairs). Even then, the risks are high. As an example, the construction of a new semiconductor plant with dust-free working spaces at Regensburg cost Siemens almost £60 million. The price of its UK Communication and Information Systems' new

headquarters at Feltham, Middx, has not been disclosed. Even the nature of the project adds to the financial risks, because development and manufacture go hand in hand. When a development team manager so advises or decides, equipment is bought, staff is engaged, or a production process is modified immediately. If he has made a mistake, that has instant financial consequences. In some instances, it may be necessary to order tools or equipment without knowing for certain whether they will be used at all.

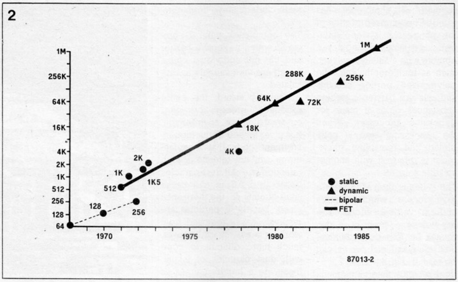


Fig. 2. The rise of solid-state memories (source: IBM).

The technology

The size of the memory cell structures used on these devices is of the order of 1.0 to 1.5 μm, so that even dust particles of only 0.5 μm can render the chip useless. Such particles can only just be observed under very powerful microscopes. The structures are etched onto the wafer with the aid of light close to the ultraviolet region ($\lambda = 0.4$ μm). When structures become smaller than 0.7 μm, they will have to be etched with the aid of X-ray lithography.

Typical of the specifications of a Mbit memory are those of IBM's proprietary device: 1 048 576 bits, divided into four blocks of 256 Kbit each, are contained on a wafer with an area of only 80.85 mm². This results in a density of 13 025 memory cells per square millimetre, so that six of these devices can contain the contents of a book of 250 pages—see Fig. 3.

The IBM device is a DRAM that needs a supply of only 5 volts. During operation, it requires a power of 0.5 W; in the quiescent mode, only 50 mW. At a temperature of 75° C, its access time is 150 ns. Its structures measure 1 μm and it is produced in FET technology. Field-effect transistors are used because their structure is simpler and they are therefore easier to manufacture.

Currently, most 1 Mbit memories are DRAMs, since static memories—SRAMs—need more transistors and therefore take up more space. Dynamic memory cells generally consist of one transistor and one capacitor, whose charge has to be refreshed at regular intervals. This is, incidentally, also the reason that DRAMs are slower than SRAMs.

It should be noted here that (magnetic) bubble memories have been available for some years in capacities of 4 Mbit (but in wafer areas of about 1500 mm²), while 16 Mbit devices are beginning to become available.

The production process

The production process of a 1 Mbit memory entails no fewer than four hundred stages. The starting point is the wafer, a thin slice of monocrystalline silicon, which has a diameter of between 120 and 150 mm, depending on the manufacturer. This wafer is used as the substrate onto which the memory cell structures are fabricated.

The memory is designed with the aid of a CAD (computer-aided design) system, which ensures that the integrated circuit conforms to its physical and electrical requirements. The information obtained from the system is used to produce the pattern on the mask. The mask is a device for shielding selected areas of the wafer. It is either emulsion on glass or an etched thin film of chromium or iron oxide on glass, and is produced by photographic reduction from large-scale layouts. The patterns are cut into the emulsion or film by electron-beam lithography.

The substrate is covered with a solution of positive photoresist by spincoating, spraying, or immersion. The desired pattern is then produced on the substrate by photolithography (after the

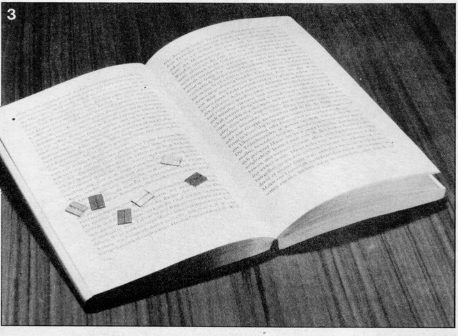


Fig. 3. Only six 1 Mbit memories are needed to store the contents of a 250 page book.

solution of photoresist has dried). The exposed portion of the photoresist is depolymerized and removed during development with a suitable solvent, such as trichloroethylene. The polymerized portion remains and acts as a barrier to etching substances or as a mask for deposition processes. When the processing step is completed, the remaining photoresist is removed with another suitable solvent.

The wafer is then etched in a dry process, which ensures uniform vertical edges. The dry-etching process also causes far less track damage than chemical etching as can be seen in Fig. 4.

Until recently, interconnexions between circuit components were also etched into the substrate. Nowadays, a number of manufacturers use a different method. The photoresist on the wafer is exposed to light through the mask and then heated: this causes the exposed portions to be preserved. The wafer is then exposed to light without the mask and developed. The portions which were covered by the mask are not preserved and disappear during the development. Finally a thin film of metal is vaporized onto the wafer: superfluous metal and the remaining photoresist are removed together.

To obtain layers with different conductivity, the silicon is doped with different ions, for instance, by implanting boron ions into the crystal lattice of the silicon. This process, carried out in a vacuum at high electric potentials, is much more precise than the usual diffusion process. A much higher packing density then becomes possible, the switching behaviour becomes more reliable, and cross-talk is much reduced.

The individual transistor elements are then interconnected or insulated from one another by chemical vapour deposition—CVD—of thin layers of gaseous monocrystalline silicon, silicon oxide, and silicon nitride. In this way, a dielectric of about 15 nm is formed. A number of layers is then put together with the individual metallized surfaces insulated from one another by the gettering of quartz (old method) or gaseous silicon nitride (modern method). The latter material protects the wafer more adequately from impurities.

The completed wafer is provided with a protective barrier and cut into individual chips, which are then suitably encapsulated.

As already stated, the entire production process is carried out in a dust-free environment. It is clear in view of the high investment costs that manufacturers can not tolerate a high rejection rate. All dust particles larger than 0.5 µm can cause short-circuits in the horizontal plane, but these particles are relatively easily removed from working areas. It is, however, much more difficult to cope with dust particles of 0.1 µm: these are a hundred times as common as 0.5 µm particles, are invisible, and lead to short-circuits in the dielectric of the memory locations in the vertical plane of the chip. It is worth reflecting on the fact that dust-free production spaces of Class 10 are one hundred times cleaner than any hospital operating theatre.

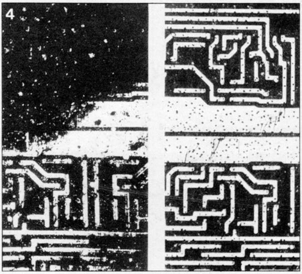


Fig. 4. Everything looks normal in the right-hand part of this picture, but the ultrasound photograph at the left-hand side shows serious damage to the interconnecting tracks.

Final test

Before the wafer is cut into individual chips, an electrical final test is carried out on any two chips simultaneously. In this, 22 needle probes many times form a connexion between chip and test equipment (see Fig. 5). The measurements thus obtained give a clear picture of the quality of the individual memory cells. Subsequently, certain test patterns are run through all the memory cells. Finally, a number of chips are taken at random from a production batch and subjected to a life test in which 100 000 hours of operation are simulated over a period of 30 hours.

Manufacturers

As already stated, a number of manufacturers already have 1 Mbit DRAMs or EPROMs in production, while others are about to commence fabrication. Only one manufacturer, Toshiba, has so far succeeded

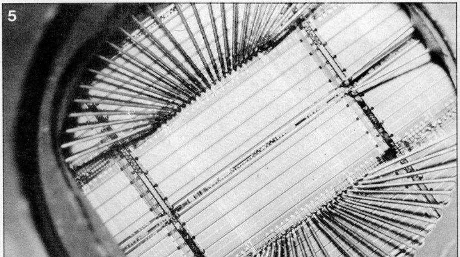


Fig. 5. During test of the completed chip, 22 needle probes scan all 1 048 576 memory cells at very high speed. (Photograph courtesy of IBM).

in producing a prototype of a 1 Mbit SRAM. The memory cell structures of this device, which is made in CMOS technology, measure only 1 μm. No fewer than 2.2 million circuit elements have been squeezed onto a substrate of only 5.99 x 13.8 mm. To be sure, the Toshiba device is both static and dynamic. Dynamic, because a refresh of the capacitor charge is necessary, and because each memory cell consists of one transistor and one capacitor. Static, because it does not need an external refresh controller (this is provided on-chip), and because it has an 8-bit bus. It is for these reasons that Toshiba calls the device a virtual SRAM, i.e. VSRAM. The device has an access time of 62 ns.

As pointed out, all DRAMs need an external refresh controller. Monolithic Memories have therefore developed controllers Type 673103 and 673104, which enable several DRAMs with access times less than 150 ns to be controlled simultaneously.

Manufacturers engaged in the development or production of Mbit memories are listed below.

AT&T produce a DRAM of 1 Mbit x 1 or 256 Kbit x 4 in CMOS technology with cell structures of 1 μm. This company started DRAM development in 1984.

Fujitsu produce a 1 Mbit x 1 DRAM.

Hitachi produce a 1 Mbit x 1 or 256 Kbit x 4 DRAM in CMOS technology with cell structures of 1.3 μm. They also produce a 1 Mbit (128 K x 8 or 64 K x 16) EPROM.

IBM has produced 1 Mbit DRAMs since April 1986. These devices are in FET technology with structures of 1 μm. All production is, however, used in IBM computer manufacture.

Intel manufactures a 1 Mbit EPROM in HMOS-II-E technology with structures of 1.4 μm and configurations of 128 K x 8 bits.

Matshushita produces a 1 Mbit DRAM in NMOS technology.

NEC manufactures a 1 Mbit DRAM in either NMOS or CMOS technology with cell structures of 1 μm. The device, which has been available since the summer of 1986, is obtainable either as a 1 M x 1 or 256 K x 4 memory. The company also produces a 1 Mbit EPROM in CMOS technology with structures of 1.5 μm. This device is available either whith a 128 K x 8 or with a 64 K x 16 configuration.

OKI produces a 1 Mbit DRAM in NMOS technology.

Philips is developing a 1 Mbit EPROM, which is anticipated to go into production early next year, as well as a 1 Mbit SRAM. Prototypes of the SRAM are expected towards the end of next year.

Siemens is developing a 1 Mbit DRAM and a 4 Mbit DRAM; the former is expected to go into production later this year. This device will have cell structures of 1.2 μm and be produced in CMOS; it will be organized as a 1 Mbit x 1 or 256 K x 4 memory. Moreover, the 1 Mbit DRAM will be manufactured as a surface-mount device

Texas Instruments is just about commencing production of a 1 Mbit DRAM in CMOS, which will also be available as an SMD (surface mount device). Cell structures are 1 μm. The company will also launch a 1 Mbit EPROM later this year which will have structures of 1.0 μm and be available in configurations of 128 K8 x 8 or 64 K x 16

Toshiba was the first producer of Mbit memories: the first 1 Mbit device was put on the market in November 1985. The device is manufactured in CMOS and is available as an SMD. Its structures are 1.2 μm. This DRAM is available as Type TC511000C-10 or TC511000-12 (see Fig. 6): the RRP of the latter is £35. These types have access times of 100 and 120 ns respectively, and require a supply of 5 V. They are driven in a similar manner as the 256 Kbit devices. The company is also launching a 1 Mbit CMOS EPROM this spring.

6

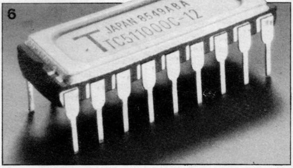


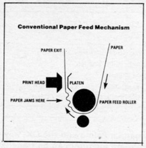
Fig. 6. This 1 Mbit DRAM from Toshiba is already available in the electronics retail trade.

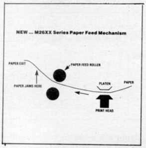
NEWS • NEWS • NEWS • NEWS • NEWS

New Epson printers

The new M26XX range of miniprinters, designed for retail and EPOS applications, features improved paper feed mechanisms, wherein the feed is after the printhead to reduce the possibility of jamming. Other benefits are fast paper feed (20+ lines/second), and a quiet paper feed mechanism, easy-to-change ribbon cassette, and 1-line validation. The new printers are very reliable and need no coin barrier as the paper exit is not vertical.

The illustrations show that with conventional paper feed mechanisms paper jams inside the machine if the paper exit is obstructed and on-the-spot attention is difficult. With the paper feed roller positioned after the print head, paper jamming can only occur at or near the paper exit and so can easily be cleared.





The new printers measure 164 x 215 x 159 mm and accept paper up to 44.5 + 44.5 mm wide. The M2630 has 17 + 17 columns, a 7-wire head, and a print speed of 2.4 lines per second. The M2660 has 21 + 21 columns, a 9-wire head, and a print speed of 3 lines per second.

Epson (UK) Ltd
Dorland House
388 High Street
Wembley HA9 6UH

REMOTE CONTROL IN ASTRONOMY

by Dr Paul Murdin, Royal Greenwich Observatory

Light from quasars and galaxies in distant regions carries messages about the beginnings of the universe. But perceiving it is difficult unless telescopes are sited on mountain tops to avoid interference from scattered artificial light. Astronomers have taken the first steps in operating such telescopes from data centres and remote control rooms instead of travelling the world to distant mountains. This is not just a matter of economy: it brings advantages of efficiency and new opportunities.

Astronomers who study radiations which cannot penetrate the Earth's atmosphere are used to operating their telescopes remotely. They have had to, for such telescopes have been carried on board satellites orbiting the Earth. The International Ultraviolet Explorer (IUE) operated by the European Space Agency tracking station from Madrid, the European X-ray Astronomy Satellite operated from Darmstadt, Germany, and the Infra Red Astronomy Satellite with its ground station in the Rutherford Appleton Laboratory at Chilton, near Oxford, are all satellites in which UK astronomers have played an active part and to which remote observing techniques have been applied.

It is not so clear why a telescope on the ground has to be remotely operated. Until recently, most telescopes have been near the astronomers' bases and could be operated by the astronomers travelling to them. But over the last 20 years astronomers have sought out places on distant mountains as sites for their telescopes, and that is why we have begun to apply space techniques to ground-based equipment.

Why are we putting observatories on mountains, in distant countries and in relatively inaccessible places?

Quasars and galaxies which formed in distant regions soon after the origin of the universe emit light which carries messages about conditions in the so-called Big Bang. The light travels to us over times of the order of 10^{10} years, over distances of some 10^{23} km. It is considerably diluted by travelling this distance (understatement!) so, to gain information about the conditions in and after the Big Bang, astronomers have to study faint objects. Their light is perceived against a 'noise' of background light from contaminating sources such as artificial light scattered by dust and their images are blurred by passage through the Earth's atmosphere. In this difficult study, maximum information can be gained only if the faint sources can be seen with the highest contrast, as the sharpest images against the darkest sky. These are the reasons why astronomers have built telescopes in the clear air on mountain tops, far from population centres that emit light and give off smoke. British astronomers have access to telescopes in Australia, Hawaii and, most recently, the Canary Islands, far from the overcrowded industrialized areas of Europe.

Relative cost

The decision whether to take the telescope's control and operation system to the user, or the user to the telescope, depends upon the relative cost of travel and that of communications. The UK travel budget for astronomy is over £1 million per year and, as fuel becomes more expensive relative to the costs of communications bandwidth, the remote operation of a telescope becomes more cost-effective. Remote operation can also offer certain advantages to the astronomer. If the observatory is very far above sea level it might be advantageous to overcome the astronomer's inefficiency in working at an altitude where oxygen deprivation can spoil judgement. One astronomer reporting on his experience at Mauna Kea in Hawaii at 4200 metres is quoted as saying "I confused the coordinates and pointed the telescope to the wrong place to take my picture, but that didn't matter because halfway through developing the photograph in the fixer I realised I had the darkroom lights on."

The simplest observations to make remotely are those which are repetitive and which generate simple measurements. The Carlsberg Automatic Meridian Circle (CAMC) on La Palma in the Canary Islands makes observations of this kind. The instrument, jointly built by the Copenhagen University Observatory and the Royal Greenwich Observatory, is a telescope which rotates around only one axis, in a North-South plane. Its purpose is to time stars as they transit through this plane, and to measure their angle of elevation above the horizon. Effectively this measures the positions of the stars, and indeed the planets, including the one on which the telescope is mounted. Construction of a consistent model of the interrelations of the star positions, and their change from decade to decade, yields information about the motion of the Earth and the dynamics of the solar system and our Galaxy of stars. Traditionally, transit measurements have been made by noting the time a star is seen by eye to pass behind a vertical cross hair and measuring its position along the hair. In the new technique used by the CAMC, the star is imaged on to a V-shaped mask which is scanned back and forth. Starlight passing through the mask is read by a photomultiplier: the phase information in its output yields the time of transit and the duty-cycle of the signal yields the position of the star along the V. The telescope is automatically operated by two minicomputers which select stars from a priority list held on a disc, position the telescope to catch the selected star for transit, make

No. of transmissions	Data
80	2048 × 128-pixel 16-bit images
320	256 × 256-point 16-bit images
10 400	2048-pixel 16-bit graphs
21 600	24 lines × 80-character/line VDU screens
5 200	60 lines × 132-character/line printer pages

Using a 9·6-kbit/s connection between La Palma and the UK, any of the data in the table (or an appropriate mixture) can be transmitted during a 12-hour night.

the measurements and reduce the data. They monitor the atmospheric conditions and cover the telescope whenever it rains; they check for cloud and malfunctions, and they make calibration measurements on a schedule. The efficiency of the telescope is such that it measures the position of 1000 stars per night to an accuracy of 0·2 arc sec (equivalent to measuring the diameter of a 1 p coin, 20 mm, at a distance of nearly 20 km). It constructs in one year a complete catalogue of star positions which would formerly have taken a decade to observe and another decade to reduce. The CAMC operates remotely in the sense that, after it is primed at the beginning of the night, the telescope works without intervention; in fact, the astronomer operating it sleeps some distance away from it. Next step in its operation will be to gain access to its programme priorities and to the reduced data from the UK.

The longest link yet achieved in remote-control ground-based astronomy is between the Royal Observatory, Edinburgh, and the UK Infra Red Telescope (UKIRT) on Hawaii. Data streams travel by microwave link from the telescope at 4200 metres to the sea-level base at Hilo and then *via* a chain of packet switched networks across the USA to Scotland. This system, using the relatively low data rates of infrared astronomy based on point-by-point accumulation of data, instead of accumulation of images, has been successfully used for a couple of years.

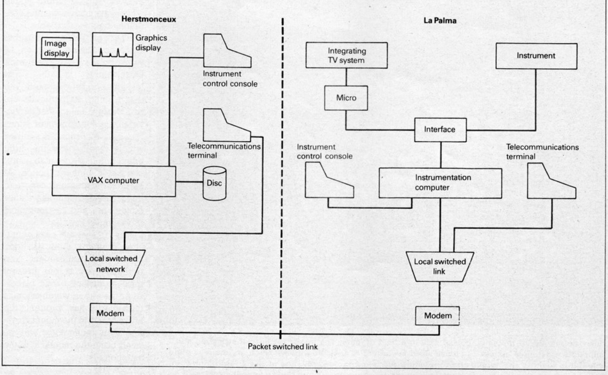
The CAMC and UKIRT generate data at low rates. Before I describe how to operate an optical telescope remotely, let us look at how it is used.

Use of telescopes

A typical large, professional telescope with a mirror of about 4 m diameter is used by some 100 astronomers per year; their experience varies enormously from student novice to professional tyro. The telescope is operated from a control desk some 10 m from the telescope by a professional telescope operator: the traditional name for this person is 'night assistant' but the radio astronomy term 'telescope driver' is also used. On a prompt from the astronomer, the night assistant causes the telescope to slew to the next star to be observed. A picture through the telescope is presented to the astronomer who then identifies in detail the object he wishes to observe and the telescope is adjusted to point directly to it. The picture is, typically, presented from a television camera viewing the phosphor of an image intensifier. On La Palma, the 2·5-m Isaac Newton Telescope operated by the Royal Greenwich Observatory uses intensified television cameras to acquire stars and the pictures can be integrated by allowing charge to accumulate on the target for several seconds before it is read, and/or by averaging successive pictures in a 512-pixel × 512-pixel × 16-bit memory. Although the picture contains half a megabyte of data, there are usually only a few significant features in it, so its information content is much less. It may be that a list of, say 10 stars, including their positions and brightness, is all that is needed to reconstruct the picture. A kilobyte will do for this.

After the telescope is positioned accurately, it is kept tracking accurately by closed-loop servos to follow the star in its rising and setting across the sky. No data is sent to any remote point in this process, which is all related locally to the telescope. But its performance is monitored by viewing reflected starlight from the entrance plate of the instrument that is being used to analyse the star, and this image is transmitted back to the astronomer. The instrument might be a spectrograph for measuring the wavelengths and intensities of spectral lines in the star. Data is produced by the spectrograph in the form of another image which is read by a detector. It would not be unusual for the telescope to follow a star and for the detector to integrate on its signal for minutes or hours. Not all this integration time is available to transmit previously-acquired information.

If the detector is an intensified television system, the signal accumulates in a memory and is available for inspection during the integration. On the basis of a preliminary analysis of a partial integration the astronomer can decide what to do: for example, he may abort because what he wants to measure is not present, or integrate until the signal-to-noise ratio of a feature hidden in the spectrum becomes large enough. The Royal Greenwich Observatory's La Palma telescopes and the Anglo-Australian Telesope located near Sydney use an Image Photon Counting System (IPCS) to record data. The IPCS fea-



Remote operations network for an optical telescope sited at La Palma.

tures image sharpening techniques and forms images made by accumulating the signals of individual photons. It is capable of generating images 2048 x 514 pixels in area and at least 16 bits in depth, and produces more data more often and with more requirement for interaction; in fact, the IPCS is the critical test for a remote operation centre.

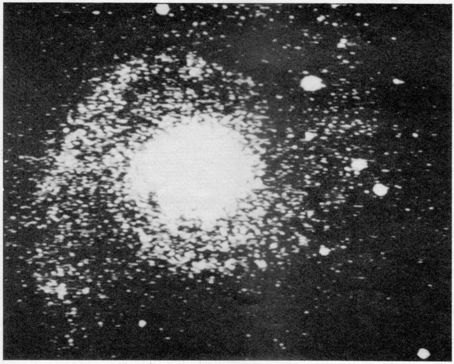
At the end of the integration the data are passed into a storage medium. Many astronomers would like, in their excitement, to begin detailed analysis immediately, and the scientific advantages are obvious: discoveries are made when the adrenalin is flowing.

Various problems

In remote operation of telescopes, each of the parts of the observing sequence presents different problems to be solved within the monetary scale set by the staff travel budget which would be saved, unlike a budget commensurate with the launch of a rocket. Positioning of the telescope is within the capacity of a low-bandwidth command channel (even of voice instruction!) and the only point of issue is safety of personnel and equipment. Altering the equipment configuration and monitoring its status also requires only a low bandwidth. Acquiring the star field, finely positioning the telescope and monitoring its position need a higher bandwidth but image condensation techniques are available to present a digest of star field to the astronomer within the 60 seconds that is the longest he will tolerate. The Kitt Peak Observatory 2·1-m telescope in Arizona can be remotely operated by what is known as a travelling operation station, which uses a video expander to receive the acquisition field after it has been compressed for transmission over telephone lines. The unit, part of an analogue device that generates, transmits and receives slow-scan pictures, was developed to meet a need for remote surveillance by security staff. Digital compression and transmission is even better adapted to high-modulation star pictures.

So, remote control of telescopes from 1000 km away is easy, a simple extension of what is already done over 10 m. The bottleneck in remote operation of optical telescopes lies in data generation: the dynamic range in astronomical data, which contains information from the very bright to the very faint, raises a problem in the process of data compression without clipping, and the analogue transmission technique used in the Kitt Peak video display is not suitable. However, over a 12-hour night with a 9·6 kbit/s connection between La Palma and the UK, any of the amounts of data listed in the table, or an appropriate mixture of them, can be sent. This is just enough to operate a productive, mountain-top optical telescope from a home station in the UK.

Once remote operation at a central home station is established, one of the next steps is to extend the number of stations, thereby making it possible to link many universities into a common programme of astrophysical enquiry, each using its specialist knowledge to interact with the data and ensure that the programme succeeds. UK astronomers already have access to a system known as Starlink, which uses nine linked computers. Some 90 per cent of British astronomers have access to this system, which provides common data-reduction software for analysing astronomical images. Once data from the telescope enters the system, hundreds of man-years worth of astronomical data reduction software can be brought to bear on it, wringing the last bit of information from the very last photon.



Television image of the spiral galaxy *M51* in a field of stars. The image is contrast-stretched and clipped so that stars appear as circles sized according to their brightness. Such an image is good enough to identify the nebula and to position the telescope on, say, one of the bright patches in the spiral arms. Its information content is much less than the original half a megabyte of data generated.

Programme flexibility

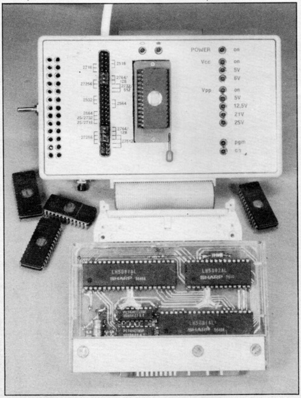
Remote operation of telescopes is stimulated by its technological timeliness, by frequently rising travel costs and by the efficiency it brings. It also affords programme flexibility. At present, astronomers are scheduled to use a big telescope for nominated nights and they use it 'come rain or shine'. Even if the sky is clear, it is largely a matter of chance whether the weather conditions are exactly matched to the type of observation the astronomer wishes to make; certain particularly critical observations may need special and infrequent conditions. It is not practical to house dozens of astronomers on a mountain for weeks at a time and move them on and off the telescope as conditions change, but if they can observe remotely, from their university offices, they can be scheduled flexibly and at short notice whenever suitable weather conditions become available.

The 4·2-m William Herschel Telescope being built on La Palma by the Royal Greenwich Observatory, is the first telescope to be designed with this in mind. Its particular optical design, called after its Victorian engineer inventor James Nasmyth, incorporates a mirror which can switch the light beam from instrument to instrument at a minute's notice. At least four instruments can stand by for development as weather conditions and astronomical programmes change.

It may be that the next generation of astronomers will look back with amusement and perhaps envy at our present travel to distant, exotic places. After the age in which avionics technology has brought the astronomers to the mountain, information technology will instead bring the mountain to the astronomers.

MSX EXTENSIONS — 5: EPROM PROGRAMMER (1)

This two-part article describes an advanced EPROM programmer intended to work with an MSX home computer. Fully supported by a tailored software package, this peripheral programmer enables MSX users to read, program and copy EPROMs with a capacity of 2 up to 64 Kbytes.



Many of the world's leading semiconductor manufacturers ostentatiously partake in the apparently unending race toward the design of ever faster and more capacious types of EPROM (Erasable Programmable Read Only Memory). Interesting as any new device in the series may be, most of us will only consider its practical use in, say, a microprocessor-based system if

1. the one-off price of the device is acceptable;
2. the device operates from a single 5 V supply;
3. the device contents can be erased conveniently with the aid of an ultra-violet (UV) light source;
4. the pin-out of the device is in line with that of its predecessors.

EPROMs nowadays come in a wide variety of types, each with its particular access time, power consumption and programming method. Though fairly exhaustive, Table 1 remains but an attempt at enumerating the most commonly encountered EPROMs. As evident from this list, there is a strong tendency among EPROM manufacturers to use *interactive programming* and lower programming voltages with increasing device capacity. Thanks to the fast progress in semiconductor technology, even the slowest of Types 2764 and up now feature an access time of 250 ns, while the use of CMOS devices is now common practice to considerably reduce power consumption and susceptibility to digital noise.

The EPROM programmer described in this article is driven by the MSX I/O and timer cartridge featured in *Elektor India*, February 1987. The first part of the present article deals primarily with the necessary hardware; next month we will discuss the software that has been written for the programmer.

Block diagram

The proposed MSX EPROM programmer is functionally set up as shown in Fig. 1. Two ports, A and B, on the I/O & timer cartridge provide the addresses for the EPROM to be programmed, while port D is used to read and write datawords. Port C drives the control interface on the programmer board. By writing the appropriate bit combination to port C, V_{CC} for the EPROM can be made 5 or 6 V, and V_{PP} can be made 5, 12.5, 21, or 25 V. Port C also controls EPROM inputs OE and CE as required for the READ, VERIFY, or PROGRAM mode of the programmer.

The CTC (Counter/Timer Controller) in the cartridge is programmed to drive a software-controlled set-reset bistable in charge of the pulse timing during the PROGRAM mode.

A jumper block is used to arrange for all programmer signals to be fed to the appropriate EPROM pins.

The logic circuits on the programmer board are fed from the computer's built-in 5 V supply. The programming and supply voltages—V_{PP} and V_{CC}—for the EPROM are available from a mains supply incorporated in the programmer.

Circuit description

A quick recap on pinning and signal denotations used for EPROMs in the 27XXX series is given in Fig. 2. It should be noted that some EPROM manufacturers—notably Texas Instruments with their 25XX types—deviate slightly from the indicated convention.

The present EPROM programmer is not a very complex circuit, as can be seen from Fig. 3. The EPROM addresses are taken from PIO Ports A and B—i.e., from IC_1 on the cartridge board. Port A provides the least significant address byte ($A_0 \ldots A_7$), Port B the most significant byte ($A_8 \ldots A_{15}$). As the "smallest" EPROM that can be programmed is the 2 Kbyte Type 2716 (or 2516 from TI), address lines $A_0 \ldots A_{10}$ are connected direct to the relevant pins on the EPROM socket. The remaining address lines appear on an extensive jumper block,

Table 1.

Manufacturer	Type	memory organization	Vpp	programming method	note(s)
AMD	AM9716	2K × 8	25 V	N	
	AM2716	2K × 8	25 V	N	
	AM2732	4K × 8	25 V	N	
	AM2732A	4K × 8	21 V	N	
	AM2764	8K × 8	21 V	N; I	
	AM2764A	8K × 8	12.5 V	I	
	AM27128	16K × 8	21 V	N; I	
	AM27128A	16K × 8	12.5 V	I	
	AM27256	32K × 8	12.5 V	I	
	AM27512	64K × 8	12.5 V	I	
Fujitsu	MBM2716	2K × 8	25 V	N	
	MBM8516	2K × 8	25 V	N	
	MBM2732A	4K × 8	21 V	N	
	MBM27C32A	4K × 8	21 V	N	CMOS
	MBM2764	8K × 8	21 V	N; I	
	MBM27C64	8K × 8	21 V	N; I	CMOS
	MBM27128	16K × 8	21 V	N; I	
	MBM27256	32K × 8	12.5 V	I	
	MBM27C256	32K × 8	12.5 V	N; I	CMOS
	MBM27C512	64K × 8	12.5 V	I	CMOS
Hitachi	HN462716	2K × 8	25 V	N	
	HN462532	4K × 8	25 V	N	
	HN462732	4K × 8	25 V	N	
	HN462732A	4K × 8	21 V	N	
	HN482764	8K × 8	21 V	N; I	
	HN27C64	8K × 8	21 V	N; I	CMOS
	HN482764P	8K × 8	21 V	N; I	OTP
	HN4827128	16K × 8	21 V	N; I	
	HN27128P	16K × 8	21 V	N; I	OTP
	HN27256	32K × 8	12.5 V	I	
	HN27512	64K × 8	12.5 V	I	
Intel	2716	2K × 8	25 V	N	
	2732A	4K × 8	21 V	N	
	P2732A	4K × 8	21 V	N	OTP
	2764	8K × 8	21 V	N; I	
	P2764	8K × 8	21 V	I	OTP
	2764A	8K × 8	12.5 V	I	
	27C64	8K × 8	12.5 V	I	CMOS
	P2764A	8K × 8	12.5 V	I	OTP
	27128	16K × 8	21 V	N; I	
	27128A	16K × 8	12.5 V	I	
	P27218A	16K × 8	12.5 V	I	OTP
	27256	32K × 8	12.5 V	I	
	27C256	32K × 8	12.5 V	I	CMOS
	87C256	32K × 8	12.5 V	I	CMOS
	27512	64K × 8	12.5 V	I	
	27513	4 × 16K × 8	12.5 V	I	Paged
Mitsubishi	M5L2716	2K × 8	25 V	N	
	M5L2732	4K × 8	25 V	N	
	M5L2764	8K × 8	21 V	N	
	M5L27128	16K × 8	21 V	N; I	
	M5L27256	32K × 8	12.5 V	I	
Mostek	MK2716	2K × 8	25 V	N	
Motorola	MCM2716	2K × 8	25 V	N	
	MCM27L16	2K × 8	25 V	N	LP
	MCM2532	4K × 8	25 V	N	
	MCM25L32	4K × 8	25 V	N	LP
	MCM68764	8K × 8	25 V	M	
	MCM68766	8K × 8	25 V	M	
	MCM68769	8K × 8	25 V	M	

Manufacturer	Type	memory organization	Vpp	programming method	note(s)
National Semiconductor	NMC2716	2K × 8	25 V	N	
	NMC27C16	2K × 8	25 V	N	CMOS
	NMC27C16H	2K × 8	25 V	F2	CMOS
	NMC27C16B	2K × 8	12.5 V	I	CMOS
	NMC27C32	4K × 8	25 V	N	CMOS
	NMC27C32H	4K × 8	25 V	F2	CMOS
	NMC27C32B	4K × 8	12.5 V	I; F2	CMOS
	NMC27C64	8K × 8	12.5 V	I; F2	CMOS
	NMC27CP128	16K × 8	12.5 V	I; F2	CMOS
	NMC27C256	32K × 8	12.5 V	I; F2	CMOS
	NMC27C512	64K × 8	12.5 V	I; F2	CMOS
NEC	µPD2716	2K × 8	25 V	N	
	µPD2732	4K × 8	25 V	N	
	µPD2732C	4K × 8	25 V	N	OTP
	µPD2732A	4K × 8	21 V	N	
	µPD2764	8K × 8	21 V	N; I	
	µPD27C64	8K × 8	21 V	N; I	CMOS
	µPD2764C	8K × 8	21 V	N; I	OTP
	µPD27C64C	8K × 8	21 V	N; I	CMOS
	µPD27128	16K × 8	21 V	N; I	OTP
	µPD27128C	16K × 8	21 V	N; I	OTP
	µPD27256	32K × 8	21 V	I	
	µPD27C256	32K × 8	21 V	I	CMOS
Rockwell	R87C32	4K × 8	21 V	N	CMOS
	R87C64	8K × 8	21 V	N	CMOS
	R27C64P	8K × 8	21 V	N	CMOS
SEEQ	2764	8K × 8	21 V	N; I	
	5133	8K × 8	21 V	N; I	
	27128	16K × 8	21 V	N; I	
	5143	16K × 8	21 V	N; I	
	27C256	32K × 8	12.5 V	I	CMOS
SGS/ATES	M2716	2K × 8	25 V	N	
	M2732A	4K × 8	21 V	N	
	M2764	8K × 8	21 V	N; I	
Texas Instruments	TMS2516	2K × 8	25 V	N; F1	
	TMS2532	4K × 8	25 V	N; F1	
	TMS25L32	4K × 8	25 V	N	LP
	TMS2732	4K × 8	25 V	N	
	TMS2732A	4K × 8	21 V	N	
	TMS2564	8K × 8	25 V	N; F1	
	TMS2764	8K × 8	21 V	N; I	
	TMS27128	16K × 8	21 V	N; I	
Thomson-CSF	ET2716	2K × 8	25 V	N	
	ETC2716	2K × 8	25 V	N	CMOS
	ETC2732	4K × 8	25 V	N	CMOS
	ET2764	8K × 8	21 V	N	
Toshiba	TMM323	2K × 8	25 V	N	
	TMM2732	4K × 8	25 V	N	
	TMM2764	8K × 8	21 V	N; I	
	TMM2764DI	8K × 8	21 V	N; I	
	TMM27128	16K × 8	21 V	N; I	
	TMM27256	32K × 8	21 V	I	
	TC57256	32K × 8	21 V	I	

The type indications as given may be followed by an access time specification.

The inclusion in this Table of PROMs and EPROMs does not imply their being programmable with the MSX EPROM programmer described in this article.

Abbreviations used in this table:

I = interactive programming.
N = normal programming (50 ms cycle).
F1 = fast programming (20 ms cycle).
F2 = fast programming (10 ms cycle).
M = Motorola programming method; not supported by this EPROM programmer.
LP = low-power device.
OTP = one-time programmable device.
CMOS = complementary metal oxide device.

Table 1. A useful list of EPROM types and their technical characteristics.

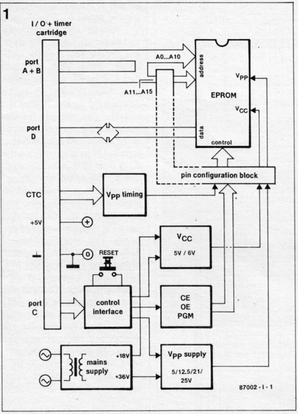


Fig. 1. Block diagram of the EPROM programmer for MSX microcomputers.

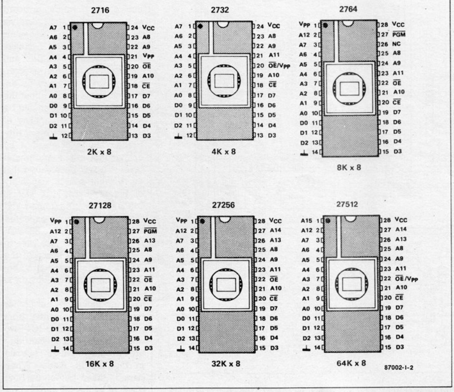


Fig. 2. Portrait of an ever growing family: pin-outs of the 2716 up to and including the 27512.

K_2, where the connections to the EPROM pins can be made as required. All address lines on the programmer board have low-value series resistors to avoid PIO outputs being damaged by a defective EPROM.

PIO Port D—i.e., IC_2 port B on the cartridge—serves to pass databytes to and from the computer. As on the address bus, protective resistors have been fitted on the $D_Ø \ldots D_7$ lines.

All programmer functions are controlled via Port C—i.e., IC_2 Port A on the cartridge. Depending on the type of EPROM in question, the correct combination of function control bits is available at Port C, bits $A_Ø \ldots A_6$.

Port C bits Ø and 1 select one of four programming voltages, 5, 12.5, 21 or 25 V. One section of dual two-to-four decoder IC_4 translates the bit pattern of $A_Ø$-A_1 into a low level at the corresponding $\overline{1YØ} \ldots \overline{1Y3}$ output, which then causes one of four voltage determining networks to be connected to the reference input of voltage regulator IC_7. Each output on IC_4 drives two open-collector (OC) TTL buffers; one to enable current to flow through the associated resistors R_{24}-R_{34}; R_{25}-R_{35}; R_{26}-R_{36} or R_{22}-R_{37}, and one to drive the associated V_{pp} indication LED. Example: writing $V_{pp}Ø=1$ and $V_{pp}1=Ø$ to the programmer causes IC_4 to activate output $\overline{1Y1}$, LED D_8 to light and IC_7 to output 21 V with R_8-R_{26}-R_{36} and the resistance of the OC output of buffer N_7 determining the output voltage. The operation on V_{pp} regulator IC_7 will be reverted to in due course.

As some of the more recently introduced EPROMs require V_{cc} to be raised from 5 to 6 V during interactive programming, provision has been made to enable the computer to select either one of these voltages as appropriate. Port C bit 3, via inverter N_6, selects either R_{33}-R_{11}, or parallel network $R_{33}+R_{11}//R_{31}+R_{32}+R_{OC(N5)}$ to determine V_{out} of IC_6. The former condition is brought about by the output of N_5 being high ($A_3=1$; $V_{cc}=5$ V); the latter by the output being low ($A_3=Ø$; $V_{cc}=6$ V). LEDs D_3 and D_4 clearly show the presence of the currently selected value of V_{cc}.

Port C bit A_2 switches V_{pp} on or off, and bit A_4 does the same for V_{cc}.

Port C bit A_5 determines the logic state of EPROM input $\overline{OE}$ (output enable), which must be low during READ operations. A two-LED indication, D_{12}-D_{13}, shows the data direction, ie., from the computer to the EPROM (PROGRAM), or vice versa (READ, VERIFY).

Port C bit A_6 controls $\overline{CS}$ (chip select) of the EPROM. Diodes D_{16}-D_{17} and pull-up resistor R_{30} are an AND gate to ensure the correct driving of the $\overline{CE}/\overline{PGM}$ pin on EPROM Types 2532, 2564, 2732, 27256 and 27512. As with $\overline{OE}$, V_{pp}, $A_{11} \ldots A_{15}$ and PGM/$\overline{PGM}$, signal $\overline{CS}$ appears on jumper block K_2 to ensure that every EPROM pin is driven with the appropriate logic level.

Port C bit A_7 is the only one set for operation as an input line. The control program running on the MSX computer checks for the presence of a logic Ø on this line, whose state is controlled with push-button S_1. Depression of this switch causes the program to halt and return to the main menu. Pressing CRTL and STOP on the computer returns control to the BASIC interpreter.

Pull-up resistors have been fitted on all Port C control lines to

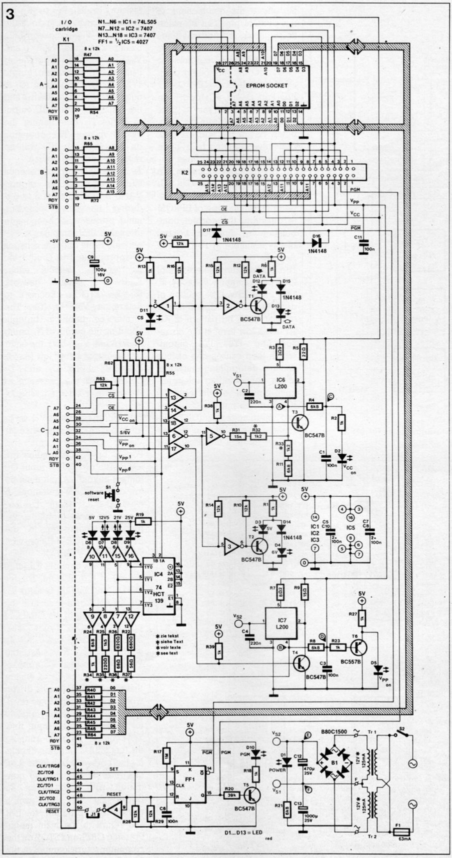


Fig. 3. Circuit diagram of the EPROM programmer, which is driven by the I/O and timer cartridge featured in our January issue.

ensure a correct bit-configuration at power-on. The V_{cc} and V_{pp} supplies on the programmer board are essentially identical circuits based on the well-known Type L200 regulator. Port C bits A_2 and A_4, when high, cause T_4 and T_3 to be driven hard by OC buffers N_{17} and N_{18}, respectively. In this manner, the current sense input of the associated regulator chip is pulled to ground, causing the IC to turn off its internal output driver. The "hard shut down" arrangement is simple and effective to ensure the absence of overshoot on the V_{pp} and V_{cc} lines. Fig. 4 shows this quite evidently. The output voltage of V_{pp} regulator IC_7 was programmed to step from 5 to 25 V with V_{pp}-off intervals between successive steps. The test was carried out with a Type 2732 plugged into the programmer. The V_{cc} and V_{pp} supplies are short-circuit resistant and can supply 100 and 50 mA, respectively, as defined with R_3 (IC_6) and R_7 (IC_7). Decoupling capacitors C_1 and C_3-C_{11} afford protection against spurious voltage transients on the V_{cc} and V_{pp} lines. Both supplies have an on/off indicator to enable users to spot defective EPROMs at a glance.

The 5 V supply for all logic circuits on the programmer board is taken from the cartridge via K_1 pins 21 and 22. This means that the computer actually feeds both the cartridge and the programmer from its internal 5 V supply. As already explained in the article about the MSX cartridge, users should be well aware of the capacity of this supply, and take every precaution not to overload it by connecting the peripheral boards. It will be recalled that the current source capability of the standard MSX slot is **300 mA**. The programmer and the cartridge can be expected to draw a total of 100 to 250 mA, but it is none the less wise to actually measure this with the aid of a regulated supply, before connecting the boards to the MSX slot.

The programming pulses for the EPROM are obtained from S-R (set-reset) bistable IC_5. Two units in the CTC in the cartridge are programmed to operate in the TIMER mode. When started, timer output Ø (TOØ) is set up by the software to provide a 4 μs delay to ensure that EPROM data and addresses are stable before activating the PGM/$\overline{PGM}$ line. CTC output TOØ is also applied to the CLK input of the second timer in the Z80-CTC package. This timer is started at the first zero count of timer Ø, and its output period is of the order of 0.5 ms, since the programmed divide factor is 7×256. The third timer in the CTC is programmed to operate in the counter mode and counts a variable number of 0.5 ms pulses at its input. In next month's final part of this article we will revert to the practical use of the software-driven PGM pulse generator. For now, it is readily seen that the timing out of the third counter causes the S-R bistable to be reset. The Q and $\overline{Q}$ outputs of IC_5 are made available on jumper block K_2 (PGM; $\overline{PGM}$), and LED D_{10} provides an indication for the presence of the programming pulses.

The EPROM programmer has a built-in power supply of conventional design delivering the raw input voltages for the V_{cc} and V_{pp} regulator circuits. There are a few rather important considerations for this supply, and these will be discussed in the following section. In conclusion of this circuit description, it is seen that the bit-configuration of Port C lines $A_0 \ldots A_6$ is specific to the type of EPROM plugged into the ZIF socket. The appropriate control word for each programmable EPROM will be given in next month's instalment. For now, the jumper configurations on K_2 are given in Table 2.

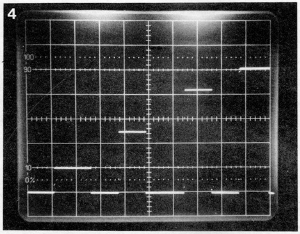


Fig. 4. The turn-on and turn-off characteristics of the L200 in position IC_7 ensure the absence of overshoot on the V_{pp} line.

Construction

The EPROM programmer is constructed on ready-made, through-plated circuit board 87002—see Fig. 5. It is a fairly densely populated board, but its completion should not present too many problems if the soldering is done with care and precision. To save board space, all resistors, except $R_{31} \ldots R_{37}$ incl. are mounted vertically. The L200 regulator chips can do without heatsinks.

It is essential to start the fitting of parts with those **at the track side of the PCB**, i.e., all LEDs, the jumper block, and the ZIF socket (consult Fig. 5, these parts are shown in dashed lines). Depending on the en-

Table 2.

K2 pos.	K2 signal	2716	2516	2732	2532	2764	2564	27128	27256	27512
1	n.c.									
2	$\overline{CE}$		$\overline{CE}$							
3	PGM	$\overline{CE}$/PGM	PD/PGM							
4	V_{pp}	V_{pp}	V_{pp}							
5	$\overline{OE}$	$\overline{OE}$								
6	$\overline{CE}$					$\overline{CE}$		$\overline{CE}$		
7	$\overline{OE}$					$\overline{OE}$		$\overline{OE}$	$\overline{OE}$	
8	A_{11}			A_{11}		A_{11}		A_{11}	A_{11}	A_{11}
9	$\overline{CE}$/PGM			$\overline{CS}$/PGM					$\overline{CE}$/PGM	$\overline{CS}$/PGM
10	V_{pp}			$\overline{OE}/V_{pp}$						$\overline{OE}/V_{pp}$
11	V_{pp}				V_{pp}					
12	A_{11}				A_{11}		A_{11}			
13	$\overline{CE}$/PGM				PD/$\overline{PGM}$		PD/$\overline{PGM}$			
14	A_{12}						A_{12}			
15	V_{cc}	V_{cc}	V_{cc}	V_{cc}	V_{cc}		V_{cc}			
16	$\overline{OE}$	n.c.	n.c.	n.c.	n.c.		$\overline{S1}$			
17	$\overline{OE}$	n.c.	n.c.	n.c.	n.c.		$\overline{S2}$			
18	V_{pp}	n.c.	n.c.	n.c.	n.c.		V_{pp}			
19	$\overline{PGM}$					$\overline{PGM}$		$\overline{PGM}$		
20	V_{pp}					V_{pp}		V_{pp}	V_{pp}	
21	A_{12}					A_{12}		A_{12}	A_{12}	A_{12}
22	A_{13}					n.c.		A_{13}	A_{13}	A_{13}
23	A_{14}								A_{14}	A_{14}
24	A_{15}									A_{15}
25	n.c.									

Table 2. Two blocks of jumpers suffice to select a wide range of EPROMs.

closure type you have in mind for this project, two corners of the board may have to be cut as shown on the component overlay.

The connecting leads of the ZIF socket, K_2 and the LEDs must be left long enough to enable the devices to protrude from the enclosure top lid. Think well before mounting the ZIF socket; it is not easy to remove once soldered onto the double-sided board. A Textool ZIF (zero insertion force) socket is undoubtedly the best to choose, and it is conveniently soldered onto two 14-way socket terminal strips soldered onto the PCB. A 28-way wire-wrap socket is also a feasible way of bridging the distance between the board surface and the enclosure top lid.

The mains parts, S_2, Tr_1, Tr_2 and F_1 are not accommodated on the programmer board, and should, therefore, be fitted with the usual care in dealing with wires and terminals at mains potential. These parts will have to find their way in some of the left over space in the enclosure. Resistors $R_{31} \ldots R_{37}$ incl. are preferably mounted in a 14-way IC socket to facilitate exchanging any of them should this be required to reach the appropriate regulator output voltage —see Fig. 7.

As you may have noticed from studying Table 2, the connections on K_2 are made in blocks of three and four. This has been so arranged to make it possible to use only two "large" jumpers for the setting of all possible configurations. Simply glue together three and four jumpers and you will have very little difficulty in finding the correct configuration on K_2 for your

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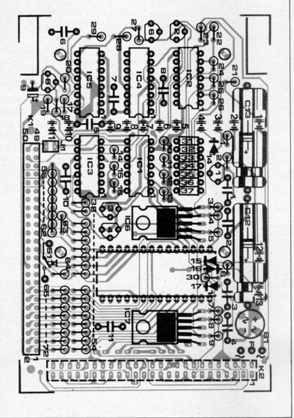

Fig. 5. Component mounting plan of the EPROM programmer. Note that dashed parts are mounted at the track side of the PCB.

Parts list

Resistors (±5%)

R_1;R_2;R_6;R_{13};R_{18};R_{19};R_{23};R_{27};R_{38};R_{39} = 1K0
R_3 = 3R9
R_4;R_8;R_{11};R_{21};R_{24} = 6K8
R_5 = 22R
R_7 = 8R2
R_9 = 15R
R_{10};R_{12};$R_{14} \ldots R_{16}$;$R_{28} \ldots R_{30}$;$R_{40} \ldots R_{72}$ = 12K
R_{17} = 1M0
R_{20} = 39K
R_{22} = 680R
R_{25} = 1K5
R_{26} = 820R
R_{31} = 15K
R_{32};R_{33} = 1K2 *
R_{34} = 1K0 *
R_{35} = 220R *
R_{36} = 68R *
R_{37} = 56R *

* See text

Capacitors:

C_1;C_3;$C_5 \ldots C_8$;C_{10};C_{11} = 100n
C_2;C_4 = 220n
C_9 = 100µ; 16 V radial
C_{12} = 470µ; 25 V axial
C_{13} = 1000µ; 25 V axial

Semiconductors:

B_1 = B80C1500
$D_1 \ldots D_{13}$ incl. = LED red
$D_{14} \ldots D_{17}$ incl. = 1N4148
IC_1 = 74LS05
IC_2;IC_3 = 7407
IC_4 = 74HCT139
IC_5 = 4027
IC_6;IC_7 = L200
$T_1 \ldots T_5$ incl. = BC547B
T_6 = BC557B

Miscellaneous:

F_1 = 63 mA delayed action.
K_1 = 50-way male PCB edge connector (angled type).
K_2 = 50-way male PCB edge connector (straight type).
7 off jumpers for K_2.
S_1 = push-to-make button.
S_2 = SPST mains switch.
Tr_1;Tr_2 = 12 V; 1.2 VA mains transformer. *
Suitable ABS enclosure, e.g. OKW 9409111.
PCB Type 87002 (see Readers Services).
28-way ZIF socket for EPROM (e.g. Textool 28).
Fuseholder for F_1.
* See text

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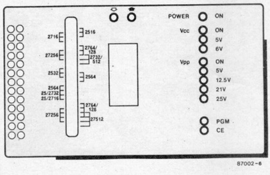

Fig. 6. Suggested lay-out for the programmer's top panel.

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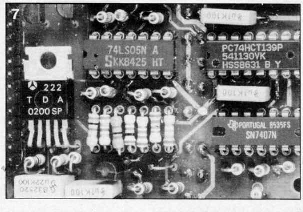


Fig. 7. Close-up of the set of voltage-determining resistors $R_{31} \ldots R_{37}$.

specific EPROM type.

In order to make for a neat appearance of the completed programmer, its top lid can be lettered as shown in Fig. 6. The connection of the programmer to the I/O & timer cartridge is made in a 50-way flat ribbon cable. A clearance should be cut into the relevant side panel of the programmer enclosure for the connection to K_1.

Testing and setting up

As all essential functions of the programmer have one or two LEDs to indicate the current state, the testing of the completed peripheral can be done largely with the aid of software. Plug in the I/O & timer cartridge into the MSX slot, but do not yet connect it to the programmer, whose internal supply must first be tested. Switch on S_2 and measure V_{S1} and V_{S2}. **It is very important that V_{S2} is less than 40 V under all circumstances. If necessary, use another set of mains transformers to prevent damaging IC_7.**

Now connect the programmer to the cartridge, and switch on the computer, which should boot up as normal. Check for the presence of +5 V on the programmer board, and measure the voltages at the test points indicated in the circuit diagram.

Proceed with keying in the test program shown in Table 3. It will allow you to see each LED on the programmer to go on and off upon the pressing of a particular function key. This is what the whole set-up should do if the circuitry functions correctly:

1. At power-on, these LEDs should light (default state):
   V_{pp} = 5 V (D_6);
   V_{cc} = 5 V (D_3);
   DATA IN (D_{13})
   POWER (D_1).
2. Running the test program causes the MSX function keys to do the following (RESET aborts the program):
   - F1 = drive successive address lines high;
   - F2 = drive successive datalines high;
   - F3 = pulse PGM/$\overline{PGM}$ for 50 ms (temporarily fit jumper J1 at output of N_4);
   - F4 = toggle V_{cc} = 5 or 6 V
   - F5 = step V_{pp} = 5; 12.5; 21; 25 V;
   - F6 = force default functions;
   - F7 = toggle $\overline{CE}$;
   - F8 = toggle data flow direction ($\overline{OE}$);
   - F9 = turn V_{cc} on/off
   - F10 = turn V_{pp} on/off

Measure V_{cc} and V_{pp} during this test to see whether any one of R_{32}...R_{37} needs adapting to enable IC_6 and IC_7 to output the correct voltages. Adapt R_{33} if the V_{cc} supply fails to output exactly +5 V, then check the +6 V level by pressing F4; slightly adapt R_{32} if necessary. Measure all four values of V_{pp} to see whether the stated resistor values in the R_{34}...R_{37} positions result in the correct output of IC_7. Make small changes at a time to all voltage determining resistors, and if possible use high stability types to get V_{cc} correct to within 0.1 V, and V_{pp} to within 0.5 to 1 V.

Next time

The concluding part of this article will be published in next month's issue. As already stated, we will then concentrate on the software for the programmer. It is our intention to make this available to you in the form of a programmed EPROM Type 27128, which should be plugged into the EPROM socket on the Add-on Cartridge Board for MSX computers, described in the March 1986 issue of this magazine.

AR

```
10 '================================================= TEST PROGRAM EPROMMER
20 '
30 '======================================================== address-area
40    A=3*16
50    DA= 4+A : DB= 5+A : DC= 8+A : DD= 9+A
60    CA= 6+A : CB= 7+A : CC=10+A : CD=11+A
70    T0=12+A : T1=13+A : T2=14+A : T3=15+A
80 '=================================== port a.b and d as output (mode 3)
90    OUT CA,255 : OUT CA,0 : OUT CA,7 : OUT CA,3
100   OUT CB,255 : OUT CB,0 : OUT CB,7 : OUT CB,3
110   OUT CD,255 : OUT CD,0 : OUT CD,7 : OUT CD,3
120 '========================== port c with 7 outputs and 1 input (mode 3)
130   OUT CC,255 : OUT CC,128 : OUT CC,7 : OUT CC,3
140 '=============================================== reset configuration
150   OUT DA,0 : OUT DB,0 : OUT DC,255 : OUT DD,0
160   OUT T2,5 : OUT T2,1
170   OUT T0,3 : OUT T1,3 : OUT T2,3 : OUT T3,3
180 '==================================================== initialisation
190   ON KEY GOSUB 290, 340, 360, 390, 420, 450, 470, 500, 530, 560
200   FOR I=1 TO 10 : KEY(I) ON : NEXT
210   ON STOP GOSUB 280 : STOP ON
220   A=1 : B=1 : C=255 : D=1
230 '==================================================== execution loop
240   OUT DA,A : OUT DB,B : OUT DC,C : OUT DD,D
250   IF INP (DC) < 128 THEN 280 : '====================== reset pressed?
260   GOTO 240
270 '=================================================== on stop routine
280   STOP OFF : GOSUB 450 : OUT DC,C : END
290 'Rotate address line high ============================ key 1 routine
300   KEY(1) OFF
310   IF A=128 THEN A=0 : B=1 : ELSE A=A*2
320   IF B=128 THEN B=0 : A=1 : ELSE B=B*2
330   KEY(1) ON : RETURN
340 'Rotate dataline high ================================ key 2 routine
350   KEY(2) OFF : IF D=128 THEN D=1 ELSE D=D*2 : KEY(2) ON : RETURN
360 'One program pulse of 50 ms ========================== key 3 routine
370   KEY(3) OFF : OUT T2,&B01010101 : OUT T2,100 : OUT T1,&B00111101
380   OUT T1,7 : OUT T0,&B00010101 : OUT T0,0 : KEY(3) ON : RETURN
390 'Vcc change ========================================== key 4 routine
400   KEY(4) OFF : C=C AND 8 : C=C+8 : C=C AND 8
410   C=(INP (DC) AND 247) OR C : KEY(4) ON : RETURN
420 'Vpp change ========================================== key 5 routine
430   KEY(5) OFF : C=C AND 3 : C=C-1 : C=C AND 3
440   C=(INP (DC) AND 252) OR C : KEY(5) ON : RETURN
450 'Reset =============================================== key 6 routine
460   KEY(6) OFF : C=255 : KEY(6) ON : RETURN
470 'Chip enable ========================================= key 7 routine
480   KEY(7) OFF : C=C AND 64 : C=C+64 : C=C AND 64
490   C=(INP (DC) AND 191) OR C : KEY(7) ON : RETURN
500 'Output enable ======================================= key 8 routine
510   KEY(8) OFF : C=C AND 32 : C=C+32 : C=C AND 32
520   C=(INP (DC) AND 223) OR C : KEY(8) ON : RETURN
530 'Vcc on/off ========================================== key 9 routine
540   KEY(9) OFF : C=C AND 16 : C=C+16 : C=C AND 16
550   C=(INP (DC) AND 239) OR C : KEY(9) ON : RETURN
560 'Vpp on/off ========================================= key 10 routine
570   KEY(10) OFF : C=C AND 4 : C=C+ 4 : C=C AND 4
580   C=(INP (DC) AND 251) OR C : KEY(10) ON : RETURN
```

87002-I-T3

Table 3. This test program uses the MSX function keys to check the correct operation of the programmer board.

BIPHASER

by W Teder

A sound effects unit that can add a new acoustic dimension to a wide variety of musical instruments.

There are various ways of obtaining the well-known *phasing* or *flanging* sound effect. Most phasers use phase-shifting networks, bucket brigade delay lines, selectively activated L-C networks, comb-type filters, or the like. The present circuit utilizes phase shifting, but has none of the drawbacks generally associated with this type of phaser, since provision has been made to obviate the troublesome amplitude-modulation effect caused by selective filtering at relatively low phaser speed settings. Where this effect is still tolerable—and often expressly sought after—with the rhythm guitar, it all but ruins the sound of numerous solo instruments, whose particular sound is not in any way embellished by appreciable volume variations. The use of a phaser based on the periodic shifting of, say, two stop-band filters results in a very lively effect with input signals relatively rich in harmonics, e.g. those of an acoustic rhythm guitar. The same phaser, however, is practically useless with a solo-instrument, since the played notes are subject to variations in amplitude, rather than in timbre.

When analysing the correlation between phasing effects and pitch of the input sound, it is noted that relatively high frequency components in the input sound typically require modulation with a correspondingly fast phase modulation signal. Similarly, the best effect for low input notes is obtained with slow phase modulation.

The foregoing considerations have been taken into account in the design of this biphaser, so named because of the use of *two* phase shifting circuits, each with its individual centre frequency and phase modulation speed control. These two circuits can be operated in parallel with two phaser speed settings to bring about a very good phasing effect without undesirable amplitude-modulation of the input signal. The circuit as presented here is but the minimum set-up of a versatile phaser unit whose controls offer a considerable variety in output sound. For those who wish to experiment a little further, there are interesting possibilities to extend the circuit to individual needs, as will be seen in the following section.

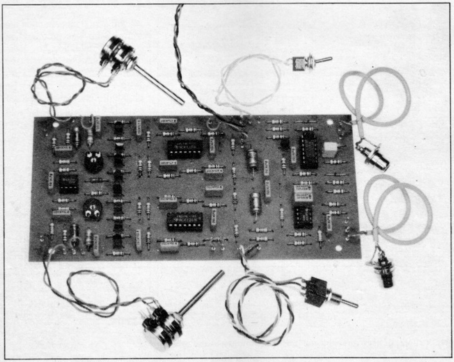
Circuit description

The circuit diagram in Fig. 1 shows that the biphaser contains the usual building blocks of an effects unit. The mono or stereo input signal is raised in amplifier A_1 and fed to two phase delaying circuits via R_{13} and R_{34}. The upper series of opamp-based all-pass filters is dimensioned for a relatively high centre frequency, while the lower series covers most of the lower part of the AF spectrum. Notice that the delay lines are identical but for the four frequency-determining capacitors, C_6-C_9 (high cascade) and C_{11}-C_{14} (low cascade). The circuits around opamps A_{11} and A_{12} are virtually identical, tunable oscillators which output a filtered triangular signal to the gates of the associated line of FETs in the delay chain.

Sufficient phase shift is obtained from both filter lines by controlling the resistances at the + input of the opamps, i.e., the resistance of the FET drain-source junction. Presets P_3 and P_4 enable a precise adjustment of the bias voltage on the gate line. The FETs in this circuit are selected for matching characteristics, to avoid the synchronicity of the opamp sections, and hence the final sound effect of the phaser, being impaired. The output signals of the PM oscillators are integrated with the aid of R_{18}-C_{10} (high) and R_{13}-C_{15} (low) to obtain sinusoidal control signals for the FETs.

Three-way switch S_1 selects the output of either one, or both, phase shifting lines. Mixing of the original input signal with the phased signal is accomplished by R_{28}, R_{49} and R_3. Opamp A_2 is the output buffer of the biphaser. The effect bypass circuit essentially consists of an optional footswitch, T_9, and a network of electronic switches, ES_1-ES_4. Since the footswitch (if used) carries a direct voltage, rather than any AF signal, its connection can be made in a fairly long, unscreened two-way cable.

One possible extension of the biphaser is the fitting of two phasing depth controls, P_5 and P_6, at the outputs of A_6 and A_{10},



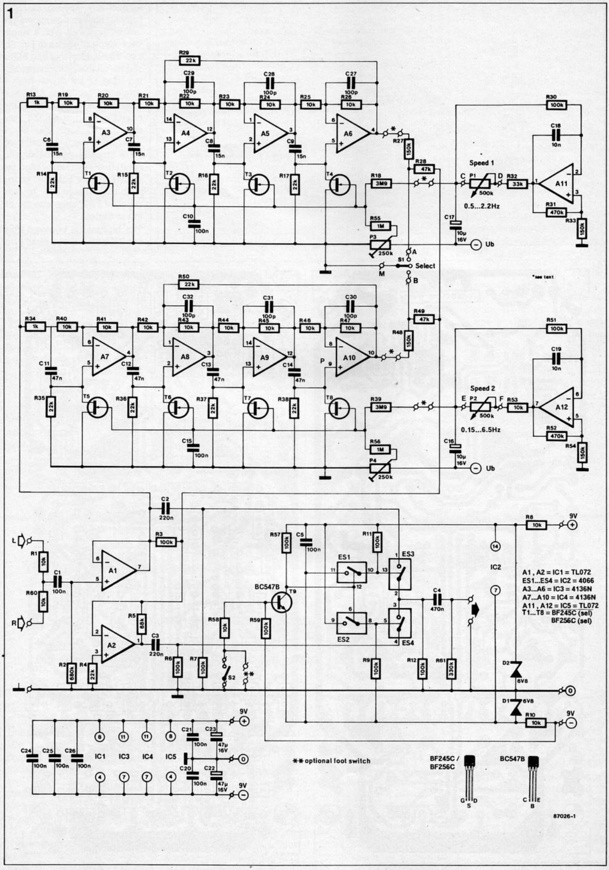


Fig. 1 At the heart of the biphaser are two individually modulated phase delay lines.

Parts list

Resistors (±5%)

R_1;R_8;R_{10};R_{19} . . . R_{26};R_{40} . . . R_{47}; R_{53};R_{58};R_{60} = 10K
R_2 = 680K
R_3;R_6;R_7;R_9;R_{11};R_{12};R_{30};R_{51};R_{57}; R_{59} = 100K
R_4;R_{14} . . . R_{17};R_{29};R_{35} . . . R_{38}; R_{50} = 22K
R_5 = 68K
R_{13};R_{34} = 1K0
R_{18};R_{39} = 3M9
R_{27};R_{33};R_{48};R_{54} = 150K
R_{28};R_{49} = 47K
R_{31};R_{52} = 470K
R_{32} = 33K
R_{55};R_{56} = 1M0
R_{61} = 330K
P_1;P_2 = 500K linear potentiometer
P_3;P_4 = 250K preset
P_5;P_6 = 100K linear potentiometer *
P_5 = 100K stereo potentiometer *

* Use is optional; see text.

Capacitors:

C_1;C_5;C_{10};C_{15};C_{20};C_{21}; C_{24} . . . C_{26} = 100n
C_2;C_3 = 220n
C_4 = 470n
C_6 . . . C_9 = 15n
C_{11} . . . C_{14} = 47n
C_{16};C_{17} = 10μ; 16 V
C_{18};C_{19} = 10n
C_{22};C_{23} = 47μ; 16 V
C_{27} . . . C_{32} = 100p

Semiconductors:

D_1;D_2 = zenerdiode 6V8; 0.4 W
IC_1;IC_5 = TL072
IC_2 = 4066
IC_3;IC_4 = 4136 (Texas Instruments)
T_1 . . . T_8 incl. = BF245C or BF256C *
T_9 = BC547B

Miscellaneous:

S_1 = SPDT with centre position.
S_2 = SPST (or foot switch; see text).
Suitable enclosure.
2 off 9 V batteries, or a mains supply.
3 off 6.3 mm jack sockets.
PCB Type 87026 (see Readers Services).

* See text.

respectively—see Fig. 2a. Alternatively, the two potentiometers can be replaced with a single stereo type as shown in Fig. 2b. The wire links at one end of R_{18} and R_{39} enable both phase shifting lines to be driven from a single PM oscillator. A further, more radical, extension of the circuit could involve the construction of additional phase delay lines, each dimensioned for a specific pass-band, and controlled by an associated oscillator. If you consider trying this out, remember to use matched FETs only, else the effort is useless.

The biphaser is powered from two 9-V batteries or a small sym-

3

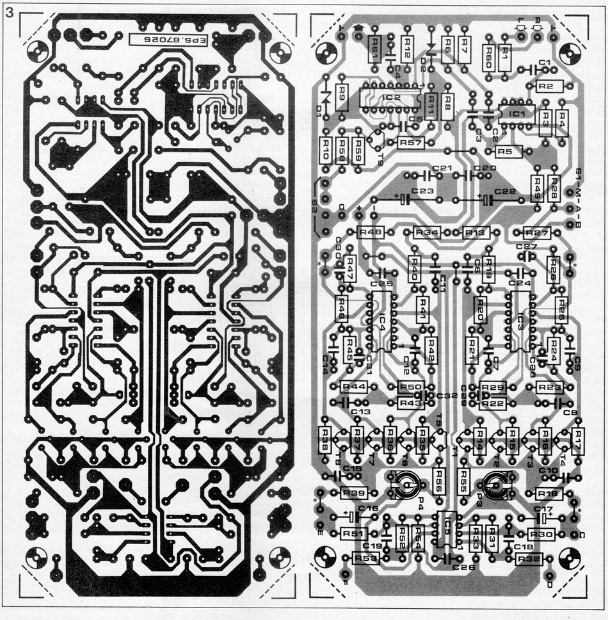


Fig. 3 Overlay diagram and track pattern of the PCB for the biphaser.

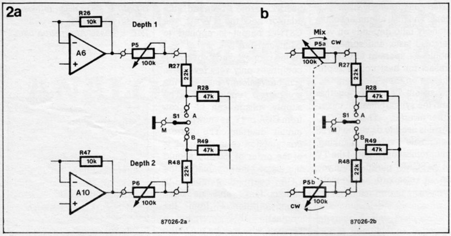


Fig. 2 Possible extensions of the biphaser.

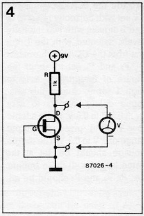


Fig. 4 Perform this current source test to select FETs with matching characteristics.

metrical mains supply. The positive and negative supply rails are adequately decoupled with C_{20}-C_{26} to prevent any likelihood of noise or hum being picked up. Current consumption of the unit is of the order of 40 mA on each 9 V supply rail.

Construction and setting up

There is virtually nothing to say about the construction of this effect unit. Hardly anything can go amiss if you stick to the Parts List and the component overlay shown in Fig. 3. The AF input and output of the phaser, as well as the foot switch input, are best made with insulated jack sockets, as customary with effect units. The enclosure must, of course, be quite sturdy, and it is recommended to use one of the smaller types of Eddystone diecast boxes, the top lid of which can be used to fit the footswitch and the speed controls. Alternatively, the biphaser can be incorporated in a mains-operated, remote-controlled effects unit, together with a fuzzer, a reverberation/echo unit, and the like, which can all be controlled from a set of footswitches on the stage.

The completed unit requires no alignment other than setting presets P_3 and P_4 for an acceptable phasing rate at a minimum of distortion. This is best done with the aid of an oscilloscope and an AF sinewave generator set to about 1 kHz at 1 V_{pp}. Connect the generator output to either one of the phaser inputs, and use the scope to monitor the phaser output signal. Adjust P_3 and P_4 for optimum amplitude modulation, i.e., the FETs should operate over the full excursion of the sinewave, without appreciable offset and/or clipping. Remove the sinewave input signal and use a voltmeter to check whether all inputs and outputs of the opamps in the phase delay lines are at about 0 V with respect to ground.

Finally, Fig. 4 shows how to select FETs for nearly identical characteristics with the aid of a simple test circuit. The FET under test is connected as a current source, and the drain-source voltage is monitored to find devices dropping the same voltage across the drain resistor.

D

SCART ADAPTOR FOR IBM PC

As a growing number of colour TV sets come with a SCART input, many owners of an IBM PC will have toyed with the idea of using a SCART compatible set as a CGA-driven, medium-resolution, RGB display. Well, here is the adaptor circuit to do just that!

Medium and high-resolution RGB monitors with TTL-compatible monitors are generally recognized as costly devices. It is not suprising, therefore, that many an owner of an IBM PC or PC compatible starts wondering about driving the video and sync circuitry in a modern colour TV set with the TTL signals from the CGA (colour graphics adaptor) in the computer. After all, the resolution of the typical TV set should be adequate for the 320×200 pixels from the CGA. Considerable difficulty, however, arises from the fact that the CGA composite video output supplies a NTSC signal (American TV standard), rather than a PAL signal as required for most European TV sets.

The solution to the above problem van be found in the use of the SCART input on the TV set; what is required is an add-on interface to convert the TTL levels from the CGA outputs to SCART levels. The vertical synchronization and the horizontal centring adjustments in the TV set will need to be slightly re-aligned to obtain a stable image from the computer. When the TV set is to remain suited for normal broadcast reception, it is suggested to fit a separate set of image adjustment controls aligned for the IBM video standard. A simple switch then makes it easy to select the appropriate setting.

Circuit description

The TTL-to-SCART level converter is shown in Fig. 1. Those readers wishing to familiarize themselves with the SCART standard and its technical characteristics, are advised to read *SCART adapter*, in *Elektor India*, October 1985.

In the proposed circuit, the level conversion is essentially from digital (Ø=0 V; 1=5 V) to analogue. Three identical level shifters, based around $T_1 \ldots T_6$

provide the SCART-compatible TV set with correctly rated R, G, and B signals with two intensity levels, selected with the I output from the CGA. With presets P_1, P_2 and P_3 set to about the centre of their travel, a logic high I input causes the analogue colour outputs to vary from 0.3 V to 0.6 V, while a logic low I input gives an output range of 0 V to 0.3 V. The toggle voltage should be set at the same level for all three buffers, i.e., P_1, P_2 and P_3 should be adjusted for identical wiper positions. The final alignment of the intensity ratio depends on your personal taste, and some time should be spent in turning the presets for best colour reproduction on the TV screen.

Transistors T_7 and T_8 together form the synchronization mixer-buffer-inverter. The CSYNC signal is used to drive the CVBS (composite video, blanking, synchronization) input of the TV set via SCART pin 20. When you use a standard, male-male, SCART cable between the adaptor and the TV set, the CSYNC output is applied to connector pin 19.

As the proposed adaptor circuit comprises only very few parts, it is conveniently built into the computer enclosure. The supply voltage can be taken from CGA pin 7, as shown in the circuit diagram. The current consumption of the adaptor is of the order of 150 mA; should this exceed the capability of the CGA board—they come in various forms and are often slightly different from the original IBM version—a separate wire may be run to the +5 V bus line on the motherboard, or a Type 7805 regulator may be used to provide the supply for the SCART adaptor board.

Finally, Figures 2 and 3 summarize the connection between CGA and computer monitor, and the pin assignment of the SCART connector, respectively.

D

IBM and IBM PC are registered trademarks of International Business Machines, Inc.

NTSC = National Television System Committee.
PAL = Phase Alternation Line.

Parts list

Resistors (±5%):
R_1;R_5;R_9;R_{14};R_{15};R_{16} = 2K2
R_2;R_6;R_{10} = 100R
R_3;R_7;R_{11} = 39R
R_4;R_8;R_{12};R_{17};R_{18} = 47R
R_{13} = 2K7
R_{19} = 56R
R_{20} = 68R
P_1;P_2;P_3 = 2K5 preset

Semiconductors:
T_1;T_3;T_5 = BF451
T_2;T_4;T_6;T_8 = 2N2219(A)
T_7 = BC547B
D_1;D_2;D_3 = 1N4148

Miscellaneous:
K_1 = 9-way sub-D plug
K_2 = 21-way angled SCART socket

We regret that no ready-made circuit board is available for this project.

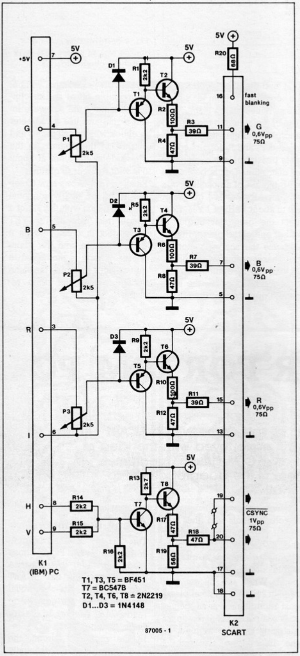


Fig.1 Only a handful of commonly available components are needed to make this TTL-to-SCART adapter for the IBM micro.

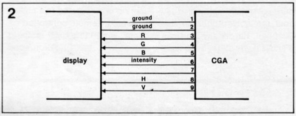
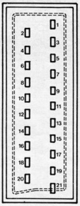


Fig. 2 Connection between CGA and RGB computer monitor.

3

SCART connector



pin	function	nominal amplitude
1	audio output (R)	0.5 V_{rms}
2	audio input (R)	0.5 V_{rms}
3	audio output (L)	0.5 V_{rms}
4	audio ground	
5	B input ground	
6	audio input (L)	0.5 V_{rms}
7	B input	0.7 V_{pp} in 75R
8		
9	G input ground	
10		
11	G input	0.7 V_{pp} in 75R
12		
13	R input ground	
14		
15	R input	0.7 V_{pp} in 75R
16	fast blanking	3 V
17	CVBS ground	
18	fast blanking ground	
19	CVBS output	1 V_{pp} in 75R
20	CVBS input	1 V_{pp} in 75R
21	connector shield	

Fig. 3 Pin assignment and voltage level convention of the standardized SCART connector.

SOFTWARE FOR THE BBC COMPUTER — 4: ANALOGUE CIRCUIT DESIGN

Anyone who has ever designed any kind of electronic circuit knows that this should essentially involve the following steps:

1. enumeration and classification of object circuit functions, and the definition of the minimum performance level;
2. finding the appropriate building blocks to realize the set funcitons;
3. make an on-paper design of the interconnected blocks;
4. building a test set-up with various measuring points readily accessible;
5. using measuring equipment to verify the required performance, make corrections, and locate the critical sections in the circuit;
6. returning to step 3, or possibly step 2, to re-assess the functioning of the various circuit sections, until the test set-up functions satisfactorily.

If only it were that simple! In practice, circuit design involves a rather more complex process, which is one of continuous feedback, re-dimensioning, the replacement of complete circuit sections, and a good deal of awareness in spotting ever better components for a particular function. Time and again it will happen that target technical characteristics prove unattainable because of component specification or cost, but also because the designer is at a loss how to get the most out of a specific circuit. It is then necessary to first build this particular section for closer analysis with the available test equipment. Textbooks are consulted, calculations are made, and the circuit is re-worked until one finds its performance to be adequate.

Although often relatively simple circuits, filters and amplifier stages, or a combination of these, are notorious for their rather unpredictable in-circuit behaviour. Calculating their performance is one thing, making them function as required is quite another. Obviously, the dimensioning of these circuits in a test set-up is a tedious and time-consuming task, which requires due attention to be paid to all variables in question, and, more importantly, the way these interact.

The widespread use of the microcomputer has brought to many designers the possibility to simulate circuits under development. This means that the actual building of the circuit involved can be done with confidence after the computer has made a prediction about the relevant technical qualities. Just how well-founded that prediction is depends on a great many factors, such as the precision of the calculations, the number of component parameters taken into account, and the "awareness" of the program that components are never ideal.

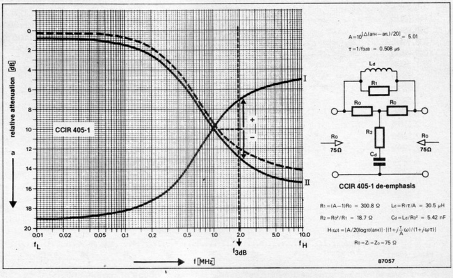
Until a few years ago, *computer-assisted design (CAD)* was only possible on professional computer systems (mainframes), mainly because of the speed and complexity of the parameter calculations performed in recursive programs. SPICE was one of the first programs for linear circuit analysis to become available for use on mainframes. As designing a circuit on a computer is in fact making a theoretical analysis of the dynamic characteristics on the basis of available component specifications, it is readily seen that any programming session initially entails the definition of in-circuit junctions, called *nodes*, connecting reactive networks, active components, etc. After running a considerable number of matrix-comparison routines, the computer is able to analyse, for instance, the frequency characteristic of the circuit in question. The complexity of the calculations, the size of the parameter library, and the required precision all determine the amount of computer memory required, and the final computation time. If the CAD program provides the possibility to closely simulate the actual behaviour of components, the results obtained are very useful for testing in a real circuit.

In the following sections we will discuss two programs for linear circuit analysis, and take the opportunity to show you how these can be used to reduce design time by having the computer do the necessary thinking before the user is confident about putting a practical version together.

Analyser II

Analyser I and *II* are BASIC programs available for many home computers. Analyser I is the simpler of the two, offering less freedom of component selection as compared with version II. Graphics presentation is not available with *Analyser I*.

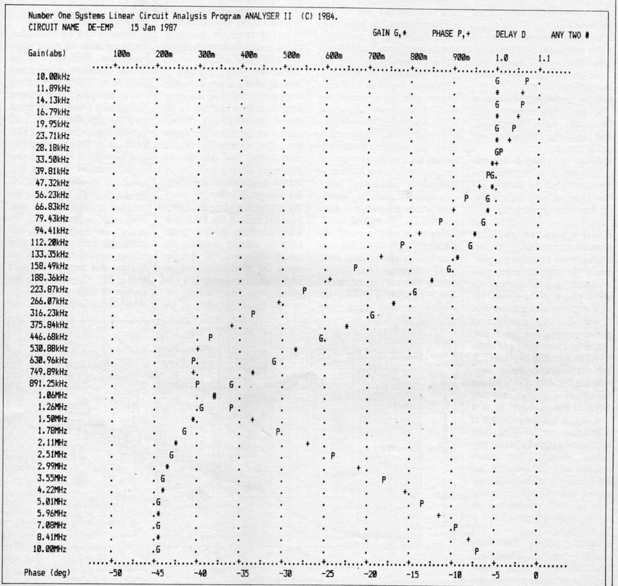
Suitable for running on any BBC Model B or Master computer, with or without a second processor installed, *Analyser II* is based on the use of BASIC types I, II, or IV. Modifying the program as required is a relatively simple matter; for instance, we could readily replace the time & date input routine by one that reads the relevant data from the Master's built-in RTC. Depending on the amount of memory in use for other programs, *Analyser II* can



Circuit diagram, design data and object response (II) of the filter under test.

```
Number One Systems Linear Circuit Analysis Program ANALYSER II  (C) 1984

CIRCUIT NAME  DE-EMP  15 Jan 1987

     Component list:

              nodes
L1            0        2       3.3E-5
R1            0        2       300
R2            0        1       75
R3            1        2       75
C1            1        3       5.43E-9
R4            3        4       20
R5            2        4       75
P             0        2       4

TEST RESULTS

       Frequency        Gain(dB abs)      Phase (deg)
        10.00k           -5.22m            -1.58
        14.13k          -10.41m            -2.23
        19.95k          -20.74m            -3.15
        28.18k          -41.26m            -4.44
        39.81k          -81.84m            -6.25
        56.23k         -161.41m            -8.75
        79.43k         -314.89m           -12.16
       112.20k         -602.21m           -16.64
       158.49k           -1.11            -22.19
       223.87k           -1.95            -28.43
       316.23k           -3.20            -34.46
       446.68k           -4.83            -39.03
       630.96k           -6.73            -40.97
       891.25k           -8.65            -39.72
         1.26M          -10.37            -35.56
         1.78M          -11.70            -29.58
         2.51M          -12.61            -23.17
         3.55M          -13.16            -17.38
         5.01M          -13.47            -12.68
         7.08M          -13.63             -9.10
        10.00M          -13.71             -6.45
```

The component values and circuit nodes are neatly summarized before Analyser II starts printing the results of the simulated sweep.



Attenuation and phase shift of the de-emphasis filter as functions of the input frequency (Analyser II).

handle up to 30 nodes and 100 components. It computes both the amplification and the phase shift of the object circuit over a user-defined frequency range. Provision has been made for the presentation of a linear or a logarithmic scale, while the frequency can be stepped in various increments to ensure the necessary resolution. Initially, the results of the test sweep are presented in the form of a table, but the menu allows the dumping of a graph on a printer, which need not necessarily be Epson compatible, as *Analyser II* outputs data by means of standard characters. Group delay as well as input and output impedance calculations are also available to the user of *Analyser II*.
The program is remarkable for its ability to take into acount that various components have parasitic reactances invariably present at terminals. A transistor, therefore, is not considered an ideal switching device, but rather a complex network of resistance and capacitance. Similarly, any inductor's parasitic capacitance is fully observed in filter response calculations, while the difference between the use of, say, a 741 or a LF356 opamp in an amplifier design becomes evident from the program output data. *Analyser II* also enables users to enter additional component parameters taken from data sheets. The computer's disc facilities are used to create an extendable filing system to hold component data, which are then instantly available for trying out in a particular circuit simulation. FETs, transformers, inductors, chokes..., *Analyser II* has got them all stored on disc and ready for use in various ratings. The available sweep band extends from 0.01 Hz to 1.1 GHz. Unfortunately, the program does not provide for the analysing of DC settings in the circuit. However, any change in the bias condition of, say, a transistor is recognized by *Analyser II*, which promptly corrects the stray capacitance figure to ensure a faithful simulation of what would undoubtedly happen in practice: a different frequency response!
In conclusion, *Analyser II* is an efficient and user-friendly program that will require a minimum of effort on part of the user to familiarize himself with the extensive range of commands and options available. A slightly unusual feature of the program is its presentation of the frequency axis in the sweep curves, but this merely requires some getting used to. The documentation supplied with *Analyser II* is an excellently detailed 25-page manual.

AC Circuit Analysis Program

This program from Markie Enterprise can only run under BASIC II because of its direct calling of routines in the BASIC ROM. It is, however, possible to run this program on the Master computer by loading BASIC II from disk into SRAM, and selecting the language as the default by means of *CON. LANG (the manual supplied with AC Circuit Analysis does not mention this trick).
This program can handle a maximum of 372 components. The calculated results appear in the form of a curve on a MODE Ø screen. Unlike *Analyser II*, *AC Circuit Analysis* is written specifically for the BBC computer, and makes good use of its function keys. The menu comprises a HELP file which makes it easy to determine one's whereabouts in the program, and provides an instantaneous overview of available program options. Unfortunately, the package does not comprise a simple cardboard template for quick reference to the various functions called up by the function keys.
A regrettable fact about *AC Circuit Analysis* is its limited range of components that can be used in the simulation. There are, for instance, only three transistor types to choose from. Whether or not this works out to be a serious disadvantage depends mainly on the applications you have in mind; for work on passive filters, the program is probably hard to beat. Unfortunately, the addition of components, the library can not be extended by the user.
The graphics offered by this program are of excellent quality, giving the impression of working with an oscilloscope-like instrument. It is possible to store a complete screen onto disk, while a screendump can be made with the aid of, for instance, DUMPOUT 3. The printer need not be Epson-compatible.

A practical case

In order to compare the performance of the two previously introduced programs, we had them analyse a number of circuits, simple as well as fairly complex ones, including the EBU de-emphasis filter incorporated in the Elektor Indoor Unit for Satellite TV Reception (see *Elektor India*, December 1986). The printouts in this article should give you some idea of the results obtained with the linear circuit analysis packages.
Although the filter under test is a fairly complex type, both programs did not require too much time to calculate the response. Therefore, the effect of changing a particular component is obvious the moment the printout is available. What does the parasitic capacitance across the inductor do to the filter response? How can the roll-off be made sufficiently steep without causing too great a phase shift? What is the expected overall attenuation of the filter, and how should it be terminated? Does it have any spurious pass-bands which could lead to oscillation in the amplifier connected to the filter output? These are but a few of the vast range of questions that can be answered by studying the output plots from the CAD programs discussed in this article. Both the makers of *Analyser II* and *AC Circuit Analysis* will no doubt be able to supply you with more information, so just write to them at the addresses given below.

Analyser II costs £51.75 incl. of VAT, and is available from Number One Systems Limited • 9A Crown Street • St Ives • Huntingdon • Cambridgeshire PE17 4EB. Telephone: (0480) 61778 (IBM, Spectrum, and Amstrad versions also available).

AC Circuit Analysis costs £60.00 incl. of VAT, and is available from Markie Enterprises • 17 Percy Road • Shepherds Bush • London W12 9PX.

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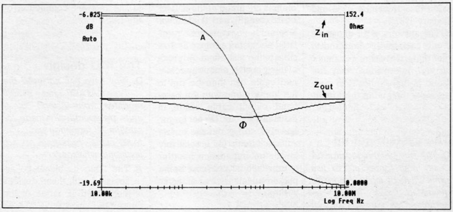


AC Linear Circuit Analysis in action. Note that the curves are written with the printer switched to graphics mode.

SATELLITE TV RECEPTION: YOUR QUESTIONS ANSWERED

by J & R v. Terborgh

With the growing interest in domestic reception of signals from geostationary TV satellites, but with many aspects of the subject still surprisingly hard to find in various publications, this article is a round-up of questions, simple ones and complicated ones, and associated answers, clear and to the point.

The reception of satellite TV services is a subject encompassing so many aspects of electronics, mechanical engineering, applied telecommunications, and other fields of interest, that it is not surprising to have baffled quite a number of readers, both those who are actually in the process of building the Elektor IDU, described over the past few months, and those who take a general interest in following any publication that has something to do with the present subject-matter.

But to begin with, a few points must be made expressly clear.

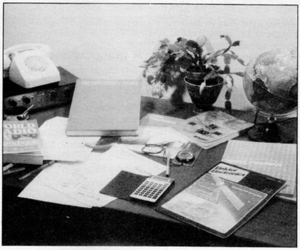
1. Depending on the specific aspects raised in the questions, these—and the associated answers—are dealt with in separate sections in this article.
2. The following convention applies concerning references to earlier articles on satellite TV reception in *Elektor Electronics*:

[A]: *Satellite TV reception*, September 1986;
[B]: *Indoor unit for satellite TV reception, parts 1, 2, and 3*; October 1986, November 1986, and January 1987.

3. The answers to all questions are necessarily short and to the point. In many instances, further information can be found in the publications mentioned at the end of this article.

The system set-up

Q. *The only suitable location for my dish forces me to use some 25 m of fairly expensive downlead coax, which introduces an attenuation of 11.5 dB at 1750 MHz. Will this impair reception?*



A. It certainly will. In general, cable losses between the LNB and the IDU should not exceed about 4 dB. Long runs of low-loss—i.e., fairly rigid—coaxial cable tend to be costly as well as cumbersome to install permanently, requiring quite a bit of digging and drilling before the signal is available at the IDU input.

A possible solution to your problem is the fitting of the IDU RF board (see [B]; part 1) into a waterproof, temperature regulated enclosure as close as possible to the dish stand. A length of inexpensive, multi-way screened cable can then be run to the home, along with the baseband output cable, made in RG58 or TV coax. Do not forget, however, to lay out the tuning voltage circuit for a relatively low output impedance, in order to prevent hum and noise being picked up (steer clear of mains wiring!).

Q. *I intend to use an older type LNB which requires to be fed with 18 V, but not over the downlead cable. Any modifications required in the IDU?*

A. Regulator IC_8 can be replaced by an 18 V series regulator circuit based around the L200 or 78GU, provided it is fed with a separately obtained input voltage of about 24 V. Remove L_1 and run a separate supply cable from point +LNB on the PSU/vision/sound board to the relevant connection on the LNB.

The IDU design

Q. *Why have you not used the Type AT1020 and AT3010 modules from Astec? These units are specifically made for satellite TV reception and come ready-made, requiring no adjustments whatsoever.*

A. The main disadvantage associated with these devices is the limited IF range of the converter module AT1020, which is designed to accept the LNB IF range of 950-1450 MHz, according to the satellite standards used in Northern America, where IDUs were originally designed for the 500 MHz wide 4 GHz downlink band. In practice, the use of these modules in Western Europe makes it impossible to receive transponders broadcasting above 10 GHz + 1450 MHz = 11,45 GHz. In Table 2b in [A], you can see what this means for ECS-1...

The AT3010 610 MHz IF amplifier/demodulator provides a 3 dB bandwidh of only 26 MHz, which is expected to give difficulty in proper reception of the future DBS services, which will operate with 36 MHz wide downlink channels.

Q. *What about the funny round arrows at the polarization selector switch on the IDU?*

A. Circular polarization—see [A]—offers a number of technical advantages over conventional, linear polarization. Fig. 26 shows the essential differences between these systems.

Linear polarization is either horizontal (H) or vertical (V) with respect to the earth plane, causing the $^1/_4\ \lambda$ probe inside the waveguide input of the LNB to have to be positioned as required for reception of the relevant transponder.

Circular polarization is either clockwise (cw) or counter-clockwise (ccw), and requires a specially shaped waveguide-to-PC board coupler.

At present, satellites only transmit linearly polarized signals, and LNB feeds suitable for cw/ccw operation are, therefore, still fairly uncommon units. If it is recalled that, polarization of downlink signals is essentially a method of allowing two transponders to operate at about the same frequency without causing interference at the receiving station, circular polarization has the following advantages over linear polarization:

1. co-channel station discrimination is typically 15 dB better;
2. downlink signals are less severely affected by Faraday rotation in the atmosphere;
3. depending on the construction of the LNB feed, the dish illumination, and hence the dish efficiency, is slightly improved.

It should be noted here that the use of a round LNB feed does not necessarily mean that the system can receive circularly polarized signals only: a round waveguide of specific diameter does nothing to the polarization of the incoming wave, and is, therefore, often used with steerable H-V polarizers to enable the LNB to be rotated over 90°, using a bearing ring around the feed, and a small, remote-controlled servo or stepper motor to select horizontal or vertical reception.

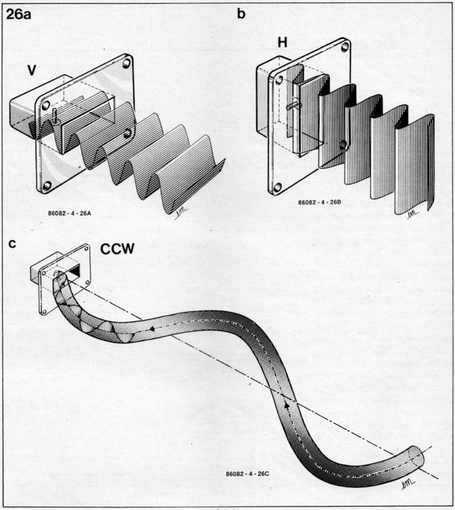


Fig. 26. Linear (H/V) and circular (cw/ccw) polarization.

Fundamentals

Q. *Why do satellites not transmit in AM, so that private reception is possible with a conventional TV set, without the need for a special FM demodulator?*

A. Transmitting an amplitude-modulated TV signal requires highly linear operation of the transponder power output stage, which must consequently be biased for class A or class AB operation, resulting in a relatively low overall efficiency. From about 5 GHz onwards, sufficient transmitter power for satellite TV services can only be obtained from travelling wave tubes (TWTs), which require to be operated in Class C at very high acceleration voltages to output a carrier power level of the order of 10-30 W at an acceptable efficiency—which is extremely important in view of the limited battery power available in the craft.

FM offers the following advantages over AM:

1. with several carriers transmitted by a single transponder, there is less likelihood of unacceptably high intermodulation products from the power output stage;
2. with a suitably dimensioned combination of pre- and de-emphasis, the obtainable S/N ratio for both vision and sound is higher at a given receiver C/n input ratio;
3. no power is wasted in the process of modulating the carrier;
4. vestigial sideband suppression is entirely irrelevant.

The fact that an FM TV system typically occupies a greater bandwidth than an AM system is of no consequence whatsoever in view of the vast capability in this respect of the centimetre-wave bands accommodating satellite TV uplinks and downlinks.

Q. *I am utterly confused by the use of terms relating to the system bandwidth. Is it true that a single satellite TV channel occupies a greater bandwidth than all short-wave bands together?*

A. Yes. There is nothing mysterious about the output bandwidth of 27 to 36 MHz required for each transponder in the satellite; it is merely the already high frequency of the modulating signal that causes the wide output spectrum. In fact, TV transponders are generally operated at a remarkably low modulation index, m' :

$$m' = \Delta f / f_{mv}$$

where Δf is the maximum instantaneous deviation from the carrier, and f_{mv} is the maximum frequency in the modulating signal causing that deviation.

With the still widely used peak-to-peak deviation of 13.5 MHz, Δf is of course 6.75 MHz, while f_{mv} is usually about 5 MHz (it will be recalled that we are dealing here with a composite colour video signal). The modulation index, m', thus works out at only 1.35. Note that sound subcarriers in the baseband spectrum are disregarded for the moment, in order not to complicate things unnecessarily.

In theory, it can be shown that the RF output signal from an FM transmitter contains an infinite number of harmonics whose amplitudes decrease as they are further away from the carrier. Without going into the complex mathematics of FM at low values of m', some 98% of the total RF energy produced by the transmitter is contained in a bandwidth, BW, written as Carson's rule:

$$BW \approx 2(m'+1)f_{mv}$$

With the previously mentioned system parameters, this gives BW = 23.5 MHz, exclusive of sound carriers, which can be expected to occupy a further 5 MHz or so.

With a tendency on part of transponder leaseholders to use relatively large values of deviation (up to 28 MHz_{pp}) so as to improve the attainable S/N ratio at limited RF power, there is, at present, increasing pressure on receiver manufacturers to give up the widely used 27 MHz bandwidth standard (for $\Delta f = 28\ MHz_{pp}$, BW works out at 38 MHz).

Q. *I am under the impression that the quality of reception offered by my receiving system is slightly improved as its gets colder outside. Why is that?*

A. Refer to Fig. 6 in [A] to see that the noise figure, F_{dB}, of your LNB is a function of its noise factor *and* the ambient temperature; the curve shown is relevant to $T_0 = 17\ °C$, but the inset calculations make it quite evident that T_r, and hence $P_{n(sys)}$, decrease with lower values of T_0 . It goes without saying that the final S/N figure is improved accordingly.

Q. *With reference to* Satellite TV reception *in the September 1986 issue, I am able to follow all the calculations from system noise to the theoretical S/N formula, (14). Yet I am intrigued by the origin of the constant, x, given as 147.3 dB for 36 MHz system bandwidth.*

A. Formula (14) is a purposely simplified evaluation of the standard S/N calculus reading

$$S/N_{(video,\ rms)} = 10\log_{10}[3/2 \cdot (\Delta f_{pp}/f_{mv})^2 \cdot BW/f_{mv}] + C/n + 13.2\ [dB] \qquad (14a)$$

in which

$S/N_{(video,\ rms)}$ = weighted, effective signal-to-noise ratio at the output of the receiver's FM vision demodulator;

Δf_{pp} = peak-to-peak deviation resulting from modulating the FM transmitter with f_{mv};

f_{mv} = highest video frequency in uplink & downlink baseband spectrum;

BW = theoretical bandwidth of transponder's output spectrum;

C/n = theoretical carrier-to-noise ratio at the input of the receiver's FM vision demodulator—see (12);

13.2 = the effect of pre-emphasis and r.m.s. weighting to CCIR Report 637-1.

The use of (14a) with parameters $\Delta f_{pp} = 13.5\ MHz_{pp}$, $f_{mv} = 5$ MHz, BW = 36 MHz, and C/n = 9.66 dB results in

$S/N_{(video,\ rms)}$ =
$10\log_{10}(78.74) + 9.66 + 13.2$ dB
$S/N_{(video,\ rms)} = 41.8$ dB.

From this it is seen that (14) is a slightly too optimistic S/N calculation, yielding the so-called *unweighted quasi-peak value*. Formula (14a), obviously more complex than (14), is the more authoritative of the two, as it is given by the EBU in Literature Reference [5].

Dish location and adjustment

Let us consider the following chicken-and-egg problem, which has puzzled many constructors of the IDU:

to be able to line up the dish aerial, one needs a fully operative receiver;

to be able to align the receiver, one needs to have the dish adjusted to "see" the satellite.

Practice does it! With a few helping hands available at the time of positioning the dish, you will find that this is not nearly as difficult as it may seem at first sight. In fact, by studying the following questions and answers, sufficient insight can be acquired to be able to go round the majority of difficulties encountered while lining up and tuning in.

Q. *I can not decide on a suitable location for my dish in the garden. Can you give an approximate indication of the maximum height of obstructions, given a specific angle of elevation?*

A. The answer to this question is best given in the form of the formula

$h = k + d \cdot \sin\alpha$
or
$d = (h - k)/\sin\alpha$

where

h = height of obstruction in line-of-sight path to satellite;

d = horizontal distance between dish and obstruction;

k = safety margin; 1 metre is recommended;

α = angle of elevation for the dish.

Especially with trees, due ac-

Table 5.

```
>LIST
   10 REM azimuth and angle of elevation for geostationary satellites
   20 DIM Orb(6):RESTORE:MODE3:REM 24x80 text only
   30 H=180/PI:REM rad-deg conversion
   40 FOR X=0 TO 5:READ Pos%:Orb(X)=Pos%:NEXT X
   50 R=6371:ALT=35822:REM See EE September 1986
   60 PRINT"*** Longitude and orbital position WEST of Greenwich: PRECEDE BY MIN
US SIGN ***":PRINT
   70 INPUT"Longitude of location ?"LO:LO=LO/H
   80 INPUT"Latitude of location ?"LA:LA=LA/H
   90 GOSUB 1000
  100 B=LO-SAT
  110 AZI=180+H*ATN(TAN(B)/SIN(LA))
  120 AZI=INT(AZI+0.5):PRINT:PRINT "Azimuth = ";AZI;" degrees  ";
  130 W$=" West of South":E$=" East of South":S$=" straight South"
  140 IF AZI=180 THEN PRINT" = ";S$:GOTO 170
  150 IF AZI<180 THEN PRINT "= ";180-AZI;" degrees ";E$:GOTO 170
  160 PRINT "= ";AZI-180;" degrees ";W$
  170 ELE=H*ATN((COS(LA)*COS(B)-R/(R+ALT))/SQR(1-(COS(LA)^2*COS(B)^2)))
  180 IF ELE<1 THEN PRINT"Satellite below horizon":GOTO 70
  190 PRINT"Elevation = ";INT(ELE+0.5);" degrees":PRINT
  200 GOTO 60
 1000 PRINT"Which satellite ?":PRINT
 1010 PRINT"1 = INTELSAT V F1/7 (FRG)         +60 deg. E"
 1020 PRINT"2 = EUTELSAT 1 F-1 (ECS-1)        +13 deg. E"
 1030 PRINT"3 = EUTELSAT 1 F-2 (ECS-2)        +07 deg. E"
 1040 PRINT"4 = INTELSAT IV A F2 (NORDIC-1)   -04 deg. W"
 1050 PRINT"5 = TELECOM F-1       (F)         -08 deg. W (not in CSS band)"
 1060 PRINT"6 = INTELSAT V F4 (UK/US)         -27.5 deg. W"
 1070 PRINT"7 = other satellite"
 1080 PRINT:INPUT"Select 1-7 --->"N
 1090 IF N>=1 AND N<=6 THEN SAT=Orb(N-1):SAT=SAT/H:RETURN
 1100 IF N=7 THEN INPUT"Orbital position of satellite --->"SAT:SAT=SAT/H:RETURN
 1110 GOTO 1080
 5000 REM geostationary arc; orbital positions East to West
 5010 DATA 60,13,7,-4,-8,-27.5


>RUN
*** Longitude and orbital position WEST of Greenwich: PRECEDE BY MINUS SIGN ***

Example: Dundalk, Ireland

Longitude of location ?-6.5
Latitude of location ?54
Which satellite ?

1 = INTELSAT V F1/7 (FRG)         +60 deg. E
2 = EUTELSAT 1 F-1 (ECS-1)        +13 deg. E
3 = EUTELSAT 1 F-2 (ECS-2)        +07 deg. E
4 = INTELSAT IV A F2 (NORDIC-1)   -04 deg. W
5 = TELECOM F-1       (F)         -08 deg. W (not in CSS band)
6 = INTELSAT V F4 (UK/US)         -27.5 deg. W
7 = other satellite

Select 1-7 --->6

Azimuth = 205 degrees  = 25 degrees  West of South

Elevation = 26 degrees
```

86082-4-T5

count should be taken of their growth and their leafing.

Q. *I live in Dundalk, Ireland, and I have a complete satellite reception system. I am, however, at a loss to understand how the dish is to be pointed at, say, Intelsat VF4. Do I have to turn it 27.5° west of south? If so, at which angle of elevation? What is the difference between azimuth and orbital position?*

A. In [A] it was already stated that there is a complex relationship between the terms raised in your question. Given the longitude and the latitude of the terrestial location, and the orbital position (OP) of the satellite, the azimuth, expressed as an angle γ with respect to the geographic north, and the associated angle of elevation, α, (see Fig. 1b in [A]), are obtained from the trigonometrical equations

$$\gamma = 180 + \arctan\left[\tan(Lo-Op)/\sin La\right]$$

$$\alpha = \arctan\left[\frac{\cos La \cdot \cos(Lo-Op) - r/(r+a)}{\sqrt{1-\cos^2 La \cdot \cos^2(Lo-Op)}}\right]$$

where
Lo = longitude of location;
La = latitude of location;
Op = orbital position of satellite;
a & r = see (1) in [A].

A pocket calculator providing the stated trigonometric functions should be set to its degree mode, and longitudes as well as orbital positions west of the Greenwich meridian should be entered with a preceding minus sign. It should be borne in mind that the result of the azimuth calculation is an angle expressed in degrees with respect to the *geographic north*, so that east, south and west correspond to 90°, 180° and 270°, respectively, similar to the indication on a magnetic compass. Depending on the specific terrestial location, there is a difference between the *geographic* and the *magnetic* north, making a compass only suitable for finding the approximate satellite position, **not** the final azimuth. None the less, a good quality compass will soon prove indispensable during the setting up of the system, as will be seen further on in this article.

Table 5 is the listing of a universal dish positioning program based upon the previously given trigonometrical calculations. Though written for the Acorn and BBC micros, the program should not be too hard to patch for other computers and their specific BASIC syntax conventions, while graphics applications may be added as required.

Since it was deemed useless to have the computer present the resulting angles with, say, 9-digit precision, lines 120 and 190 use the INT(x+0.5) instruction to attain a precision of ±0.5° for azimuth and angle of elevation, respectively. At the end of the program are 6 orbital positions given as DATA items and put into an array called POS% by the READ loop in line 40. Selection of item 7 from the list of satellites enables establishing the aerial position for services yet to be commisioned—e.g DB satellites, see Fig. 9 in [A].

With the positioning angles calculated and noted on a piece of paper, you are now nearly ready for the first practical attempt at receiving the satellite. First, however, consider the following points:

A. Your location should be within the satellite's footprint. Calculate the expected C/n ratio as set forth in [A]; if this works out as lower than +8 dB, good reception will be very difficult, if not impossible, even if all equipment is known to function satisfactorily. Very good reception requires a C/n ratio well in excess of 14 dB.

B. The dish location should offer an unobstructed line of sight to the relevant satellite. Go to the planned dish site and use the compass to find south, i.e. the needle should register with the N indication. Stand with your back to the north and imagine a horizontal line, starting from the compass pivot, across the calculated azimuth value on the dial, straight to an orientation point well removed from your position—see Fig. 27. This point may be any fairly high, well discernable object, such as a tree top, a building, a neighbour's aerial mast, a lamp post, a traffic sign, etc. Straight above this point, a considerable area of the sky should be visible, i.e. there must not be higher objects further towards the horizon. In western Europe, most satellites can be received with angles of elevation of the order of 20° to 35°, i.e. they are sufficiently high up in the sky to ensure a line of sight path with the dish mounted on a post in the ground. However, in densely built areas, it may be necessary to raise the dish well above the ground to ensure a clear view in the appropriate direction.

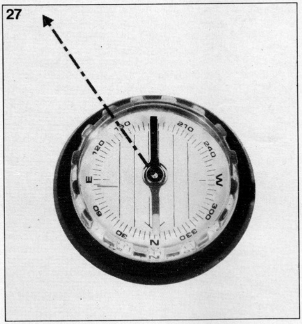


Fig. 27. Using a compass to find the approximate azimuth for the dish aerial (example).

In view of both the inaccuracy of most types of compasses, and the difference between the magnetic and the geographic north, it is recommended to first adjust the aerial elevation as shown in Fig. 28. Make sure that the protractor is held exactly parallel with the dish axis and read the angle of elevation, which is the same as α shown in Fig. 1b in [A]. With a sufficiently heavy plummet, and in the absence of gusts at the time of adjustment, the angle of elevation can be set with an accuracy of about ±1°. Owners of an offset dish or a Polar Mount system (see [A]) can not make use of the above procedure, and should consult the dish supplier for positioning instructions.

Never attempt receiving a satellite without having at least an idea of its whereabouts in the sky; it is a waste of time and rightly comparable to finding a needle in a haystack.

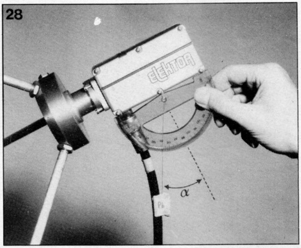


Fig. 28. Using a plastic protractor and a plummet to set the angle of elevation (example).

Upon reaching the requisite angle of elevation, provisionally lock the relevant dish adjustment(s). If the dish has a hole at the centre of its reflective surface, look through it to check whether the LNB feed is exactly on the dish axis, i.e. the feed aperture should offer optimum illumination.

Unlock the aerial azimuth adjustment(s) and make sure that the dish can revolve freely around its mounting system, without any change in the set elevation. Use the compass as explained to roughly determine the azimuth, and use the IDU SCAN facility as detailed in the section *Aerial positioning unit* in Part 3 of [B]. Turn the dish very carefully across the expected azimuth range; as the 3 dB directivity of a 1.5 metres dish is only about 1°, aiming it at the satellite is in no way comparable to adjusting, say, a UHF TV aerial! Consult Fig. 29 if you are still unsure about the difference between α and γ.

Once you have managed to see the first synchronization bars, it is a relatively simple matter to peak all dish and LNB feed controls for maximum S-meter deflection. Spend some time in finding the correct focal point for the LNB input, and see whether the polarization can be optimized by rotating the feed over a small range. Depending on the angle of elevation, there is a *polarization offset angle* to be taken into account. Especially with α smaller than 20°, it is well worth trying to establish the correct polarization offset, which may amount to $\pm 45°$ as viewed from the front of the dish.

You will probably find that manual adjustment of the dish soon becomes a routine job, and spotting various satellites within 5 minutes or so can be done with the help of two or three orientation points at a familiar location, and a few simple notes as a guide in setting the two dish angles plus the tuning dial indication on the IDU for a specific transponder.

Miscellaneous matters and the future

Q. *Apart from ECS-1 and Intelsat VF10, are there more satellites transmitting TV programmes?*

29

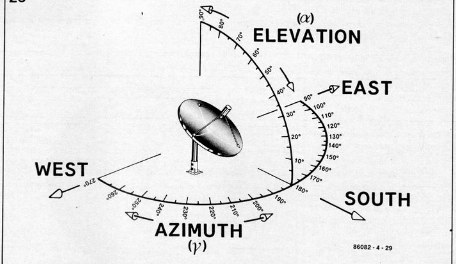


Fig. 29. To line up a dish aerial, the required azimuth and angle of elevation must be set separately.

A. Yes, there are. You may try ECS-2 at OP 7° E, which transmits three EBU newsfeed channels operated at prescheduled times and intended to provide unedited news flashes to many of Europe's national TV broadcast organizations. These transponders are also used as two-way relay stations carrying technical instructions for camera crews during important international events, such as sports, games, conferences, etc. (Eurovision Service, co-ordinated from EVC, Brussels). Also on ECS-2 is the VISNEWS newsfeed channel, and Televerket Norway, which transmits in C-MAC.

The Nordic-1 satellite at OP 4° W beams down Sveriges I and II in C-MAC.

If your location allows a wide view towards the East, you may try Intelsat VF12, nicknamed Copernicus, at OP 60° E, which is above the Indian Ocean. This satellite carries four German TV programmes, and can be received with very good quality, provided the dish elevation can be reduced to about 10° (average value in the UK).

If you are the fortunate owner of an outdoor unit comprising a Polar Mount and a steerable polarizer, it is highly interesting to spend an afternoon or so in

30

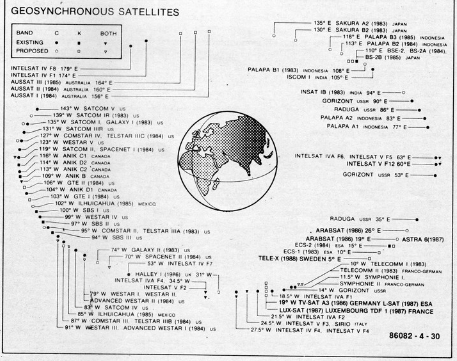


Fig. 30. Communications and TV satellites operating in the 4 GHz (C) 11 GHz (Ku) bands.

scanning the geostationary arc for further satellites; many are scheduled for launching, while existing ones are sometimes operated on an experimental basis; we have seen trial transmissions in various MAC standards, as well as test charts in encrypted video with accompanying datachannels in the audio section of the baseband. To round off this answer, Fig. 30 shows an overview of currently operative satellites; it must be noted, however, that many of these only transmit digital data for use in international business communication systems. Others have either a very low output power, or a very narrow downlink beam.

Q. *What is causing the delay in getting started with the European direct broadcasting projects?*

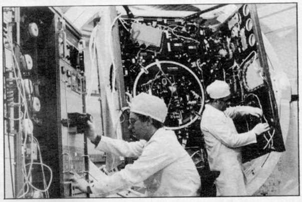
A. Although expressly promised by the French and German broadcasting organizations, last year did not see the commissioning of their joint DBS project, TV-SAT & TDF-1. In order to avoid adding to the general confusion about the future of direct broadcasting by satellite, the following points summarize the problems involved:

1. Both ESA and NASA have been forced to re-organize launch schedules because of their research into the possible cause of technical failures in carrier rockets used in attempts to put satellite payloads into orbit.
2. The final reliability of high-power TWTs providing the required output power of some 300 W still worries the engineers at Marconi, Thomson-CSF, Telefunken and G&C. Although the availability of sufficient battery power to feed the DB transponders is ensured with solar panels extending over some 20 metres, the stability of the carrier output level still does not meet the set requirements for good quality reception on earth during worst case atmospheric conditions.
3. The economic viability of DB services remains rather questionable; the follow-up projects, TV-SAT 2 and TDF-2, are now in real danger of being cancelled altogether. Also there are numerous political and commercial problems involved in finding leaseholders for the transponders on board of these craft. Meanwhile, receiver technology has not come to a standstill. Once TV-SAT & TDF-1 are operational, their huge transmit power rating may well be superfluous for LNBs with a noise figure of the order of 1.8 dB. Refer to the calculations in [A] to understand that a 1.2 dB improvement in LNB noise figure is equivalent to an EIRP increase of about 3 dB.

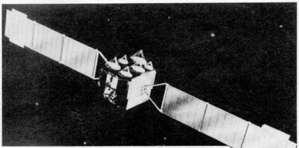
In view of the above considerations, it is not surprising to read about swift progress being made in the development of medium-power transponders. Often referred to as *quasi-DB Satellites*, a new series of orbiting craft is currently being developed. These satellites, of which the new Intelsat V FII and Eutelsat F-2 types are good examples, will hold twice as many transponders as TV-SAT 1, each producing an EIRP of about 50 dBW, enabling good reception with a 1 metre dish and an LNB with a noise figure of less than 2 dB. It will be interesting to see how these services will do as compared with the prestigious TV-SAT and TDF combination.

RTL (Radio Télévision Luxembourg) has taken the daring step of having RCA develop and build the **Astra** satellite, which is said to be a six-channel, 52 dBW type, to be positioned at OP 19° West (see Fig. 9 in [A]). It is our understanding that Astra will be operational in the summer of this year, i.e., even earlier than the Franco-German project. With our readers, we are very keen on receiving the first high or medium power signals from orbital positions assigned to DB satellites. Meanwhile, we will do our best to keep you abreast of the latest developments!

RGK;Bu



Work in progress: engineers at AEG are building and testing a section of a DB satellite.



Eutelsat 1-F1 in orbit.

Literature references:

[5]. *Direct broadcasting experiments with OTS; synthesis of results.* EBU Technical Publications no. 3231-E.

[6]. *Essential characteristics for a Eutelsat I receiving earth station having the minimum required performance for television.* EBU Technical publication no. 3248-E.

■ Various articles in *Elektor Electronics*:

Satellite TV receiving equipment, February 1986, p. 27 ff.

Electric propulsion for satellites, September 1986, p. 65 ff.

Jockeying for supremacy in Europe's own space race, October 1986, p. 36 ff.

For further reading:

■ *Satellite TV applications (ed. April 1986).* Plessey Semiconductors.

■ *World Satellite Almanac*, by Mark Long. Available from Harrison Electronics • Century Way • March • Cambs. PE15 8QW. Telephone: (0345) 51289.

■ *Satellites today. Home satellite TV installation and troubleshooting' manual. The hidden signals on satellite TV.* These books are available from Universal Electronics, Inc. • 455 Groves Road • Suite 13 • Columbus • Ohio 43232 • USA. Telephone: 614-866-4605.

■ *Fernsehsatelliten*, by Stratis Karamanolis. Available through Elektor Electronics' Book Service (£4.95).

■ Various articles in *EBU Review (technical)*:*

Pan European DBS project-Europa TV, by F Kozamernik (no. 215).

The C-MAC/packet system for direct satellite television, by H Mertens & D Wood (no. 200).

The performance of C-MAC in a hardware simulation of a DBS transmission chain, by P Shelswell (no. 212).

Satellite transmitter powers for DBS, by G J Phillips (no. 216).

* A catalogue of technical publications can be obtained free of charge from European Broadcasting Union • Technical Centre • Att. M. Systermans • Avenue Albert Lancaster 32 • B-1180 Brussels • Belgium.

Nothing generates quite so much interest in computers by raw beginners as a computer that makes noises. This is particularly true with children and especially if the computer can actually play its own tune on command. It can encourage them to take a serious interest in programming and/or computers in general.

Junior Synthesizer

make your computer play your favourite tunes

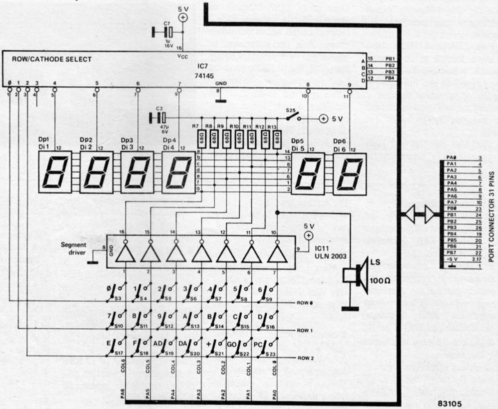
A. Bricart

When a flood of new musical instruments appeared that could be controlled by a microprocessor, some of the many Junior Computer owners must certainly have combined the two ideas. Actually this computer lends itself quite readily to controlling an analogue synthesizer. However, some people have probably not yet taught their computer to play music and so to make it easier we have written a program to turn your Junior Computer into a Junior Synthesizer.

A singing display

The only 'hardware' needed for this JC to JS conversion is a 100 Ω loudspeaker that is connected between one of the display driver outputs of IC11 and ground. No other special interface is needed as the only component used is connected directly to the existing circuit. The audio signal that feeds the loudspeaker is produced by the 6532 on the main board of the computer, and consists of a series of pulses whose frequency is determined by the software. The tune to be played is memorized in page $Ø3ØØ and is made up of a series of bytes, two of which are needed for each note to be played. The first is placed in an even address and corresponds to the pitch of the note; the second, corresponding to the duration of the note, is placed in the next odd address. The pitch depends on the frequency of the pulses, and the duration depends on how long the signal lasts.

1



There are four values of duration possible: minim, equal to two crotchets, each equal to two quavers which in turn are each equal to two semi-quavers. The durations are calculated from the computer clock which has a frequency of 1 MHz. For example, the note 'A' at 440 Hz has a pulselength of 2.28 ms. With a symmetrical waveform, the space lasts 1.14 ms. There is already a timing stage available in the computer (DELAY). So for our 'A', this delay has to be executed 81 times before inverting the logic level (81 x 14 $\mu s \approx$ 1.14 ms). Thus the hexadecimal value of the pitch of this note is $51 (81 in decimal).
Because the program is very simple, only the $Ø3ØØ page (up to $Ø3FF) can be used to memorize a melody, so it can only have 127 notes at most. The tempo is fixed by the contents of location MULT ($ØØØ2) which can be changed to increase or decrease the speed of play. The rhythm is determined by the magnitude of the bytes in the uneven addresses, although, of course, the value of the durations also varies with the pitch of the notes.
When the processor finds the value $ØØ in an even address (pitch), it is silent for a certain length of time which is normally determined by the contents of the immediately following uneven address. If on the other hand, the value $ØØ is in an uneven address the tune is stopped and starts again from the beginning.
In the example given here, the Junior plays the Menuet du Bourgeois Gentilhomme by J. B. Lully, but with a little experimentation you can probably make it play 'Chopsticks' as well! ◼

Table 1

Note	Hz	pitch code	duration code (minim)	(crotchet)	(quaver)	(semi-quaver)
E	1318.5	1B			84	42
D#	1244.5	1D		F9	7C	3E
D	1174.6	1E		EB	76	3B
C#	1108.7	2Ø		DE	6F	37
C	1046.5	22		D1	68	34
B	988	24		C6	63	31
A#	932.3	26		BA	5D	2F
A	880	29		BØ	58	2C
G#	830.6	2B		A6	53	2A
G	784	2E		9D	4E	27
F#	740	3Ø		94	4A	25
F	698.4	33		8C	46	23
E	659.2	36		84	42	21
D#	622.2	39	F9	7C	3E	1F
D	587.3	3D	EB	75	3B	1D
C#	554.3	41	DE	6F	37	1C
C	523.2	44	D1	69	34	1A
B	494	48	C6	63	31	19
A#	466.1	4D	BA	5D	2F	17
A	440	51	BØ	58	2C	16
G#	415.3	56	A6	53	2A	15
G	392	5B	9D	4E	27	14
F#	370	61	94	4A	25	12
F	349.2	66	8C	46	23	11
E	329.6	6C	84	42	21	1Ø
D#	311.1	73	7C	3E	1F	1Ø
D	293.6	79	75	3A	1D	ØE
C#	277.2	81	6F	37	1C	ØE
C	261.6	89	69	34	1A	ØD
B	247	91	63	31	19	ØC
A#	233.1	99	5D	2F	17	ØC
A	220.6	A2	58	2C	16	ØB
G#	207.6	AC	53	2A	15	ØB
G	196	B6	4E	27	14	ØA
		ØØ	E0	7Ø	38	IC
			ØØ			

Table 1. The codes for the pitch and duration of the notes shown here can make the Junior Computer play your favourite tune.

```
JUNIOR

M
HEXDUMP: 2ØØ,25D
       Ø  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
Ø2ØØ: A9 7F 8D 81 1A A9 Ø8 8D 82 1A A9 ØØ 85 ØØ A9 Ø2
Ø21Ø: 85 Ø2 A6 ØØ BD Ø1 Ø3 85 Ø1 FØ E5 A9 4Ø 8D 8Ø 1A
Ø22Ø: 2Ø 5Ø Ø2 A6 ØØ BC ØØ Ø3 FØ Ø8 A9 BF 8D 8Ø 1A 2Ø
Ø23Ø: 5Ø Ø2 C6 Ø1 DØ E5 C6 Ø2 DØ D8 E6 ØØ E6 ØØ A2 FF
Ø24Ø: CA EA EA EA DØ FA 4C ØE Ø2 ØØ ØØ ØØ ØØ ØØ ØØ ØØ
Ø25Ø: A6 ØØ BC ØØ Ø3 A2 Ø2 CA DØ FD 88 DØ F8 6Ø
```

Table 2. This is the program which uses the 6532 and the display driver to generate an audio signal that is heard through the loudspeaker. No physical alteration to the existing circuit is needed.

```
JUNIOR

M
HEXDUMP: 3ØØ,36B
       Ø  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
Ø3ØØ: 51 58 3D EA 41 DE 3D 75 36 84 51 58 48 63 5B 9C
Ø31Ø: 61 4A 5B 4E 6C 84 61 94 79 3A 51 58 3D EA 41 DE
Ø32Ø: 3D 75 36 84 51 58 48 63 5B 9C 61 4A 5B 4E 6C 84
Ø33Ø: 61 94 79 3A 61 94 5B 4E 51 BØ 51 58 48 63 48 63
Ø34Ø: 56 53 51 BØ 51 58 3D EA 48 63 41 6F 41 6F 51 58
Ø35Ø: 3D 75 3D 75 48 63 41 DE 3D 75 51 58 48 63 5B 9C
Ø36Ø: 61 4A 5B 4E 6C 84 79 74 ØØ 7Ø ØØ ØØ
```

Table 3. The sequence reproduced here corresponds to the notes and rhythm of the Menuet du Bourgeois Gentilhomme by Lully. The even addresses contain the pitches and the uneven addresses are the durations of the notes. Note that in some cases the durations are not exactly minims. The $ØØ at $Ø36B acts as a repeat bar. It indicates that the piece is to be replayed from the start.

LCD panel meter

a versatile 3½ digit display

The use of digital voltmeters as panel meters is becoming increasingly popular these days. The version described here can be used for level measuring devices, multi meters, power supplies, etc.

Digital panel meters have one major snag and that is their 'floating' input. This can cause problems resulting in display errors. The reason for this will be explained later. On the other hand, they also have many significant advantages: since they are based on ICs, they require very few external components and therefore take up little space. The IC already incorporates an automatic zero adjustment, an automatic polarity indicator, a clock oscillator and a reference voltage source. The IC used here can also drive a display, has provision for an external reference voltage, indicate an over-range and measure the input voltage off-earth (although the latter will cause problems as mentioned above). We will go into the various power supply methods later, but first let us look at the circuit itself.

The circuit

For the advantages offered, the circuit is surprisingly simple, as shown in figure 1. Only very few components are needed in addition to the 7106 IC and an LCD display. The only other active element in the circuit, the VMOS FET BS170 is merely required for the decimal point conversion and could even be omitted.

The frequency of the IC internal oscillator is determined by R5 and C2. This will be about 45 kHz here. The dual slope measurement process occurs three times per second. Readers who would like to pursue the details will find them in the article 'Universal digital meter' published in January 1979.

The automatic zero setting is adjusted by the value of the capacitor C4. It will be correct when '000' appears on the display with the input shortcircuited. C3 acts as a charge capacitor for the reference voltage during the automatic zero adjustment.

The IC contains a highly temperature-stable reference voltage source. This is about 2.8 V typ. and appears between pins 1 (+U_B) and 32 (COMMON). The reference for the integrator is derived from this voltage. The full-scale indication on the display will correspond to exactly half the reference voltage. For example: full scale → 200 mV reference voltage → 100 mV. This voltage is connected to input REF HI by way of P1. The input voltage is divided across R7/R8 into IN LO IN HI. Voltages above 200 mV can be measured when R8 has the following values: 120 k (equivalent to 2 V full scale), 12 k (equivalent to 20 V full scale) and 1k2 (equivalent to 200 V full scale). Since the voltage is not divided in a precise 1 : 10 ratio, the display indication has to be corrected with P1. Another solution would be to use a convertible input voltage divider, in which case R8 could be omitted.

The power supply

The panel meter can be powered either symmetrically or asymmetrically.

1. Symmetrical power supply: the meter input is grounded. If power provided is ± 5 V, then R1/D1 and R2/D2 are not required for stabilising the supply. At higher symmetrical supply voltages the values of R1 and R2 are calculated as follows:

$$R1 = \frac{\frac{+U_B}{V} - 4.7}{5}\ k\Omega \text{ and}$$

$$R2 = \frac{\frac{|-U_B|}{V} - 4.7}{5}\ k\Omega$$

In both cases 'B' and LN LO are connected to each other. The power supply and the panel meter both have the same ground connection.

2. Asymmetrical power supply: the meter input is 'floating' and subject to the problems mentioned earlier: the meter input can only 'process' voltage levels between 0.5 V below +U_B and 1 V above $-U_B$. If IN LO is connected to the ground of the power supply $-U_B$, input voltages have to be at least 1 V before they can be indicated . . . that is, unless the scale is adjusted. Something will have to be done to remedy this. The solution is to connect the asymmetrical supply voltage between +U_B and $-U_B$, point 'A' to IN LO, thereby causing a floating off-earth input voltage to be produced. The asymmetrical voltage can be provided by a 9 V battery which has a lifespan of about 200 operational hours at a maximum current consumption of 1.2 mA.

Construction

The printed circuit board and the component overlay are shown in figure 2 and as can be seen, it is very neat and compact indeed. IC1 should be mounted on a socket. The LCD display is placed in IC connectors on the copper side of the board. Take care — the display is very fragile! By the way, almost any type of display is suitable. A few suggestions have been given in the parts list. Readers who have difficulty spotting pin 1, should hold the display up against the light to see the position of the decimal point. The decimal point must be at the lower edge when the display is mounted. This is where the connections are marked for the decimal point ('1' . . . 'M').

Calibration

This is very straightforward. A known voltage level is connected to the input and P1 is then used to adjust the display to this value. Obviously, care must be taken to ensure that the correct measuring range was selected at the input by means of R8 or a voltage divider. Finally, the value indicated on the panel meter may be compared to that of an accurate DVM at the same input voltage. The comparison should be carried out over a period of time and any deviation should be corrected.

Using the panel meter

Right at the beginning of this article we mentioned how versatile the panel meter is. Nevertheless, if ground referenced voltages are to be measured, the power supply voltage will have to be symmetrical. If, for instance, the meter is to be used as a DVM in power supplies, a separate power supply may well have to be constructed!

If, on the other hand, the meter is to be connected to the barometer published in September, there will be no problem. The various connections are carried out as follows. The supply voltage is derived from the barometer's power supply. The $+U_B$ voltage of the panel meter is linked directly to the positive terminal of C8 and the $-U_B$ voltage is linked to the negative terminal of C9. IN HI is connected to the temperature and pressure outputs of the barometer via a switch. A second pole of the switch makes sure the decimal point is correctly positioned. A three-way switch with two poles is needed for the humidity sensor for it to be extended into a miniature weather station.

The digital barometer is calibrated in the manner described in the September issue. Afterwards, P1 in the panel meter is adjusted to allow the reference pressure value to appear on the display■

1

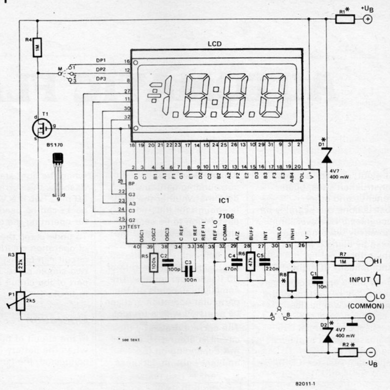


Figure 1. The panel meter circuit. It is based on the well-known 7106 DVM IC which directly drives an LCD display. The supply voltage may be selected to provide either grounded or 'floating earth' measurements.

2

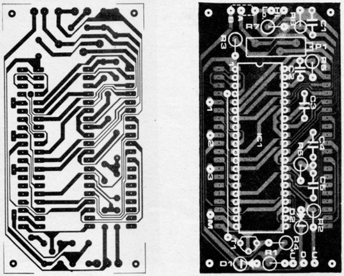


Figure 2. The printed circuit board and component overlay of the panel meter. IC1 should be mounted on a socket. The LCD display is fitted with IC connectors on the copper side of the board.

Parts list

Resistors:
R1,R2 = 2k2
R3 = 22 k
R4,R7 = 1 M
R5 = 100 k
R6 = 47 k
R8 = 120 k
P1 = 2k5 10 turn trimmer

Capacitors:
C1 = 10 n
C2 = 100 p
C3 = 100 n
C4 = 470 n
C5 = 220 n

Semiconductors:
D1,D2 = 4V7/400 mW zener
T1 = BS 170
IC1 = ICL 7106
LCD = 3½ digit (4305 R 03/data module — 3901, 3902/Hamlin — SE 6902) Standard version with 13 mm character height

AUTOMATIC FLASHER

At night, parked vehicles, construction sites, open trenches and other obstructions can scarcely be recognised. However, one can easily warn against these by using a flasher, which turns on automatically at night.

Many more applications can be thought of for this circuit and with few modifications, it can even be put to practical commercial use. The basic circuit exploits the property of light dependant resistor (LDR), which "See" the surrounding light and dermine whether the light is enough for the obstruction to be seen clearly or does it need the flashing signal. In darkness, the lamp starts flashing approximately at the rate of 60 flashes per minute. The sensitivity depends on the particular operation and can be adjusted with a trimpot.

The current drawn by the circuit is around 15 to 30 mA depending on the ambient light. In darkness, when the light starts flashing, the current rises to 50 mA. Two 4.5 V battery packs can be used in series for operating the circuit.

To understand the principle of operation clearly, the circuit can be divided into two simple parts. The first part of the circuit is shown in figure 1.

Operation

In the circuit of figure 1. when the battery is connected, the lamp L is off, but depending on values of R1 and R2, capacitor C2 starts charging. When it reaches the voltage of approximately 1.4 V, T2 starts conducting and the lamp starts glowing. Now the capacitor remains charged and lamp continues to glow. If, however, the capacitor C2 is short circuited, it quickly discharges and brings down the base voltage of T2 to the ground level. T2 stops conducting and lamp L turns off again.

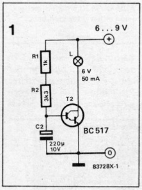
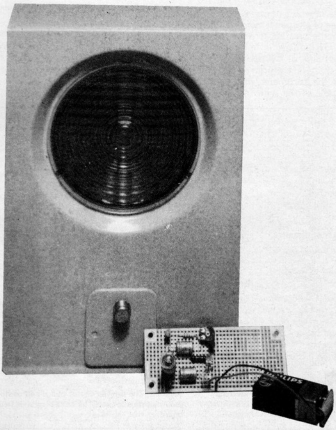


Figure 1 : The transistor goes into conduction as the capacitor C2 charges to 1.4 V, which is also the base-emitter voltage of T2.



2

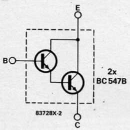


Figure 2 :
The Darlington-Transistor BC 517 can be replaced by two BC 547 B transistors as shown.

3

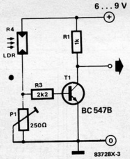


Figure 3 :
Under insufficient ambient light,the LDR has high resistance and the transistor turns off. Under lighted condition LDR has low resistance and the transistor goes into conduction.

If the short circuit is removed, then the capacitor C2 again starts charging and soon the lamp L starts glowing. The requirement of 1.4 V across base. emitter of T2 is explained by the fact that it is a Darlington Pair and thus has two base-emitter junctions in series to be fed by the base-emitter voltage. The Darlington Pair Transistors have already been discussed in detail. In case the Darlington Transistor BC 517 is not available, it can be replaced by two BC 547 B transistors as shown in figure 2.

The charging time of C2 depends on its value as well as the values of R1 and R2. Higher the value of R1, R2 and C2, the longer it takes for C2 to charge to 1.4 V.

Let us now have a look at the second part of the circuit, shown in figure 3. This is the LDR circuit. The LDR R4 has a very low value when light falls on it and gives a very high resistance in darkness When the ambient light is high , R4 is low, thus giving a high voltage on base of T1 and turning it ON. The voltage on collector of T1 is then nearly the ground voltage. As light falling on LDR is reduced the value of R4 increases. Voltage across P1 decreases and at a certain level of ambient light, T1 turns OFF. The voltage on collector of T1 is almost equal to the supply voltage.

Now combining the two parts we can construct the circuit of the flasher as shown in figure 4. The only addition required is the capacitor C1. The setting of P1 should be such that with sufficient ambient light, voltage U1 should be above 0.7 V. and with insufficient ambient light it would drop below 0.7 and turn off T1.

As soon as T1 is off, the voltage on its collector is nearly the supply voltage. C2 starts charging and voltage across C2 soon reaches 1.4 V, which turns T2 ON. Lamp L glows as soon as T2 starts conducting. This state will be maintained as long as LDR R4 is in dark. So, if we mount the LDR in such a way that the lamp L can illuminate the LDR when it glows,it will automatically turn on T1 again and subsequently turn off T2. This is due to the fact that C2 gets discharged through R2 and T1.

As soon as T2 is off, the lamp L also extinguishes, bringing back darkness. The cycle of flashing thus

4

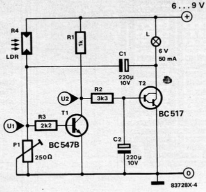


Figure 4 :
The combination of the two circuits of figure 1 and figure 2. Only additional component is C1.

begins again. The bulb and LDR combination ensures that the circuit works only in darkness and that the lamp flashes at fixed intervals. Technically this action is known as feed back coupling. The output condition of the circuit, namely the glowing and extinguishing of the lamp is fed back to the input which is the LDR. All alternating, flashing or oscillating circuits work on the principle of feed back coupling.

The flashing frequency depends on the delays introduced by C1 and C2, C1 decides the delay between turning on of lamp L and switching on transistor T1, which in turn switches T2 and the lamp off. C2 decides the delay between T1 turning off and T2 on. In short, C1 decides the ON time of the lamp and C2 decides the OFF time of the lamp. Both together, decide the time of the flashing cycle.

Construction

Most improtant aspect of the construction is that the LDR should be positioned in such a manner that when ever the lamp L is glowing, its light must fall on the LDR, In addition to this, the LDR must also be open to the ambient light. The resistance of the LDR can be between 75Ω to 300Ω under lighted condition and under darkness it can be more than 10 MΩ. If you get an LDR with different values, the setting of P1 can take carte of that. The housings of LDRs can also differ from manufacturer to manufacturer, but this would not pose any problem.

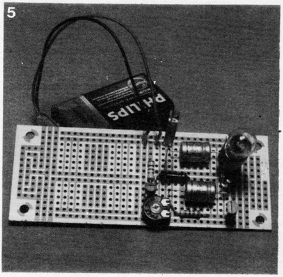
Only half of the PCB will be required to accomodate all the components. The electrolytic capacitor polarity must be correctly observed.

As indicated earlier, T2 can be replaced with two BC 547 B transistors as shown in figure 2. This alternate arrangement is shown in the component layout by dotted lines. The circuit can be made more compact by mounting the capacitors and resistors in vertical positions rather then horizontal.

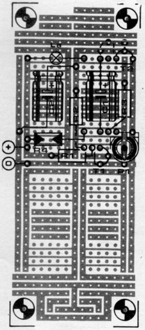
Testing

After everything has been assembled correctly, place the sliding contact of the trimpot at point U1 so that the resistance P1 becomes zero. This makes T1 off and T2 on. The lamp glows continuously. Now turn the sliding contact of P1 slowly towards earth terminal, at one position, the lamp will start flashing. Subsequently P1 should be so adjusted that the lamp flashes only when LDR is in darkness. This can be done by adjusting P1 while the LDR is covered from ambient light by hand.

5



6



Parts List
R1 = 1 KΩ
R2 = 3.3 KΩ
R3 = 2.2 KΩ
R4 = LDR
P1 = 250 Ω Trimpot
C1, C2 = 220 μF/10V
T1 = BC 547 B
T2 = BC 517
or 2 x BC 547 B
L = 6V/50mA bulb
1 SELEX PCB
1 Lamp holder
Battery pack, hook up wire etc.

Figure 5 :
The LDR should be so mounted that it receives the light from lamp L when it lights up.

Figure 6 :
Component layout on SELEX PCB. The replacement of the Darlington-Transistor by two BC 547 B is shown with dotted lines.

VOLTAGE DIVIDER IN BASIC

Formulae and equations encountered in circuit design, incite every computer enthusiast to calculate the values on his machine. A small program for doing the voltage divider calculations is presented here for those SELEX readers who are interested in computer applications.

First of all, let us refresh our memory about the voltage divider formula. The voltage across R1 is given by the relation

$$U_1 = U \frac{R1}{R1 + R2}$$

Where the fraction

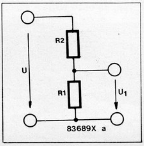
$$\frac{R1}{R1 + R2}$$

represents the actual voltage divider ratio; i.e. the factor, by which the input voltage is reduced.

The BASIC program given in figure 1 allows us to print a table with the component ratios which can be obtained with the application of E12 series resistances. The table consits of 12 columns for the E12 series values from 1 to 8.2 of the resistance R1 and 48 different R2 values from 0.01 to 82.

The lines 110 to 190 read the E12 series resistance values. Lines 200 to 240 allow the computer to write the table head. The last part of the program contains two loops. The inner loop (270 to 290) allows us to calculate the individual divider values (280) and respectively to print out a line of the table. The outer loop (250 to 310) provides the next values for R2, with which the inner loop writes a new line.

The program was written for a TRS 80 computer with an 80 column printer. The program given here will have to be modified with LPRINT in place of PRINT to get the actual printout on the printer.



If it is run as it is, the output will be only on the screen. Some more modifications may be necessary depending on the BASIC available on your computer. For those computers who do not accept 3 letter variables, the variable terms ROW and COL will have to be replaced by single letter variables. The "PRINT USING" statements also may cause problem with some computers. If this command is not recognised by your computer, you will have to replace it with a subroutine.

	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4
0.010	0.990	0.992	0.993	0.994	0.995	0.996	0.997	0.997	0.
0.012	0.988	0.990	0.992	0.993	0.995	0.996	0.996	0.997	0.
0.015	0.985	0.988	0.990	0.992	0.993	0.994	0.995	0.996	0
0.018	0.982	0.985	0.988	0.990	0.992	0.993	0.995	0.995	
0.022	0.978	0.982	0.986	0.988	0.990	0.992	0.993	0.994	
0.027	0.974	0.978	0.982	0.985	0.988	0.990	0.992	0.993	
0.033	0.968	0.973	0.978	0.982	0.985	0.988	0.990	0.992	
0.039	0.962	0.969	0.975	0.979	0.983	0.986	0.988	0.990	
0.047	0.955	0.962	0.970	0.975	0.979	0.983	0.986	0.988	
0.056	0.947	0.955	0.964	0.970	0.975	0.980	0.983	0.986	
0.068	0.936	0.946	0.957	0.964	0.970	0.975	0.980	0.983	
	0.924	0.936	0.948	0.956	0.964	0.971	0.976	0.979	
			[illegible]	0.947	0.957	0.964	0.971	0.975	
					[illegible]	0.957	0.965	0.970	
							[illegible]	0.963	

```
100 REM voltagedivider
110 R=48
120 DIM E12(R)
130 FOR ROW=1 TO R
140 READ E12(ROW)
150 NEXT ROW
160 DATA .01,.012,.015,.018,.022,.027,.033,.039,.047,.056,.068,.082
170 DATA .10,.12,.15,.18,.22,.27,.33,.39,.47,.56,.68,.82
180 DATA 1.0,1.2,1.5,1.8,2.2,2.7,3.3,3.9,4.7,5.6,6.8,8.2
190 DATA 10,12,15,18,22,27,33,39,47,56,68,82
200 PRINT"      ";
210 FOR COL=25 TO 36
220 PRINT USING"#.#"; E12(COL);:PRINT"    ";
230 NEXT COL
240 PRINT
250 FOR ROW =1 TO R
260 PRINT USING"##.###";E12(ROW);:PRINT"    ";
270 FOR COL=25 TO 36
280 PRINT USING"#.###";E12(COL)/(E12(ROW) +E12(COL));:PRINT"  ";
290 NEXT COL
300 PRINT
310 NEXT ROW
```

MOSQUITO REPELLANT

They will be swarming once again, the unwanted, winged torturers, looking for the victims and leaving behind swelling and itch! The mosquito problem is a part of everyday life, especially during the summer.

Since time immemorial, inventive people have struggled hard to find effective means of protection against these insects. Even though it is a fact that only the females are dangerous, the males can also create situations of panic by their humming. Scientists say that these and many other insects find some particular frequencies of sound very unpleasant and run away from, these frequencies.

It seems quite obvious then, that by creating these frequencies electronically, we should be able to repel these insects! The most important point to remember here is that, unfortunately, this method has so far not been completely successful. Whereas one group of insects can be made to run away at frequencies around 5 KHz, other types may desert only at higher frequencies, about 10 .... 20 KHz. For some types, all the frequencies may fall on deaf ears! Yet other theories propose that in fact some frequencies may even attract them instead of repelling.

Whatever may be the truth, trial is superior to just theorising. Even though the cost of our circuit may prove to be a wrong investment, as the population of mosquitoes and insects who are immune to our insect/mosquito repellant is likely to be predominant! The loss is not very high - four resistors, two capacitors, two transistors, and a buzzer.

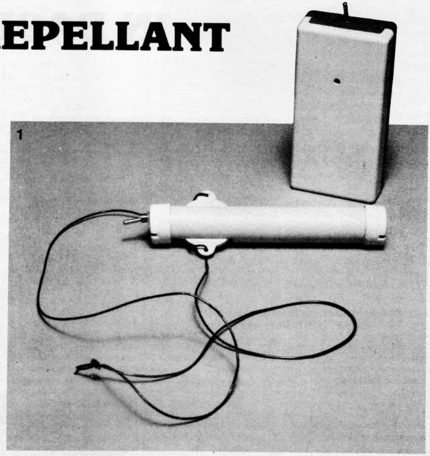


Figure 1 :

Two prototype of the Mosquito/Insect Repellant circuit. Any standard plastic box can be used. Even a plastic tube with end caps can be used.

The Circuit

The Astable Multivibrator, which is generally used as a signal generator, is once again used here to generate the desired frequencies. It is an excellent example of the fact, how versatile simple basic electronic circuits can be.

Let us quickly see ;the operation of the Astable Multivibrator circuit, shown in figure 3. When T1 is conducting, T2 is off and when T2 is conducting, T1 is off. The capacitors C1 and C2 contribute decisively to this ON/OFF cycles for the transistors T1 and T2. The time taken by C1 and C2 to charge and discharge decides the shape of the output waveform. Another important factor in the operation of the circuit is the fact that the transistor goes into conduction only when the base-emitter voltage exceedes 0.7 V (for silicon transistors). From this basic knowledge we can visualise how the transistors exchange their roles and how the voltage on the collector of each transistor jumps between the lower and upper level, producing a rectangular waveform. If you take a second look at figure 3 carefully, you will notice that C1 and C2 are not equal. They differ in their values by a factor of four. The output signal will thus be a non symmetrical waveform. Such a non symmetrical signal contains more high frequency harmonics compared to the normal square wave signal. The output of our circuit will have the basic frequency of 5 KHz along with the harmonics of 10,15 and 20 KHz. If some insects are deaf to frequencies upto 5 KHz, they may react to 10 KHz or 15 KHz or even 20 KHz, one never knows ......

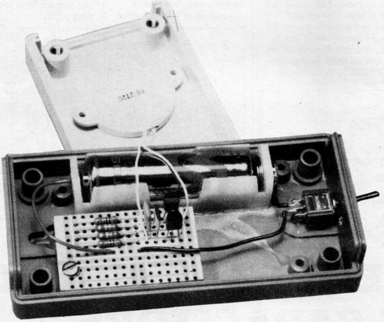
Construction

Just one fourth of the standard SELEX PCB is enough to construct the circuit. Figure 4 shows the component layout for the complete circuit. Please note that the base terminal T2 must be bent in the reverse direction through the space between collector and emitter terminals. A sleeve may be used on the base terminal to avoid accidental contact with the collector and emitter terminals.

Any suitable plastic box can be used as the casing for the circuit. Two alternatives are shown in figure 1. The Piezo-Buzzer and battery pack alongwith a switch can also be easily fitted into the casing. The Piezo Buzzer should not have an internal oscillator built into it. If the gadget is expected to be used on a beach, it must be made watertight except, of course, the buzzer opening. The circuit takes about 0.3 mA current, and can give about 1500 hours of nonstop operation.

Parts List
R1, R4 = 10 K Ω
R2, R3 = 560 K Ω
C1 = 82 pF
C2 = 330 pF
T1, T2 = BC547
1 Piezo Buzzer (without internal oscillator)
1 SELEX PCB
1 Suitable Casing
1 battery 1.5V
1 Toggle Switch.

2



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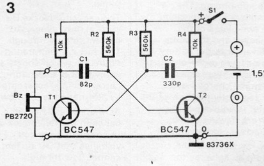

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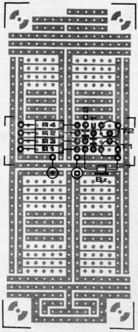


Figure 2 :
The "Acoustic Gun" employed in the circuit is a small piezo-buzzer element.

Figure 3 :
The circuit — very simple and clever.

Figure 4 :
Component layout on a standard SELEX PCB. The base terminal of T2 must be bent through the space between collector and emitter terminals.

LOGIC PROBE

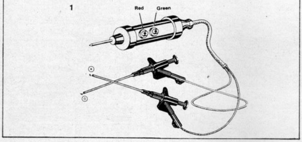
The circuit diagram shows perfectly clearly that T1 together with R3, R4, D5 and D6 constitute a current source for LEDs D3 and D4. As a result, the current to the LED will be approximately 12 mA, irrespective of the operational voltage. The LED cathodes are grounded by either N1 or N2 enabling.

The LEDs are switched on and supplied by a constant current. The circuit's other task depends on the voltage applied to the disconnected end of R1. If, for instance, a relatively high voltage with respect to the ground potential is applied, N1 will invert the 'high' level, grounding the cathode D3. D3 lights to indicate a logic '1'. But D4 remains unlit, as its cathode is 'high'. It won't light until a very low voltage (less than 1/3 of the supply signal) is applied to R1, in which case the 'low' level will be inverted twice before reaching the cathode of D4. R1, D1 and D2 protect the circuit against an input overload.

The high-impedance 10 MΩ input resistor (R2) limits the load to the circuit under test. It also cuts off the input of the first inverter N1 when the test input is disconnected. This prevents the circuit from going 'haywire', should there by any interference at the input. All the components combine to form a very effective, straightforward logic probe for TTL and CMOS signals. In TTL circuits, the logic levels displayed by the tester do not quite match their exact definition, but it should be adequate for a rough estimate. Incidentally, when pulse sequences are applied at the input of the circuit, both LEDs will light irrespective of the corresponding frequency. In other words, they will be lit continuously in most cases. The logic tester does not require its own power supply, as it operates on an 'automatic level matching' basis. That may sound complicated, but that is exactly what it does! What happens is that the operational voltage is derived from the circuit being tested. As a result, the logic probe will always respond correctly to the level in force at any particular moment.

The entire circuit can be housed in a plastic tube or even in the plastic holder of a ballpoint pen. The test 'pen' is provided with a probe at one end and two connection wires including clamps at the other. Once the two clamps are connected to the power supply of the circuit-under-test, the probe merely has to touch a test point for the LEDs to instantly indicate the correct logic level at that point.

1



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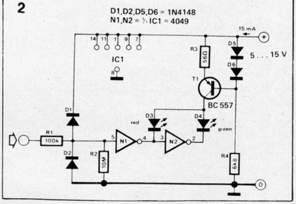


THE MEMBRANE MODEL OF CAPACITORS

Many simple electronic processes seem to be complicated because we don't actually see what is happening inside the component. Take for example the capacitor, its charging/discharging operations can be very easily explained using the membrane model.

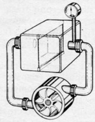
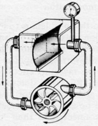
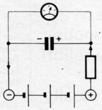
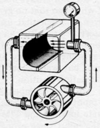
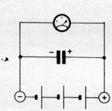
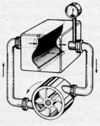
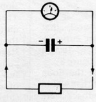
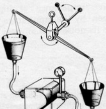
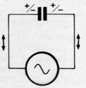
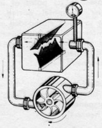
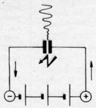
The so-called membrane model is shown in figure (a). A container is divided in two chambers by a membrane. The two chambers are interconnected externally through a pump. The chambers are equivalent to the two plates of the capacitor and the pump is equivalent to the battery. Water filled in the chambers and tubes represents electrical charge - and consequently the flow of the water is equivalent to current flowing in the capacitor - battery circuit.

The resistance in the circuit would be same as the resistance offered by the connecting pipes to the flow of water forced by the pump.

The capacitor blocks DC current, but allows AC current to flow through. This fact is illustrated in figure (e), which shows an equivalent of alternating current being represented by alternating water flow.

As there is a dielectric between the two plates of the capacitor, we can visualise that DC current cannot flow through. Alternating current flow is difficult to visualise, but it can be explained as alternate charging and discharging cycles.

This property is used in electronic circuit for separating out the DC and AC parts of a current. A capacitor in series blocks DC and allows AC. A capacitor in parallel with a signal by passes the AC to ground and allows only DC to flow through to the output.

a			(a) With equal water in both chambers, the membrane is relaxed The membrane separates the two chambers.	In uncharged condition, the capacitor voltage is zero, Dielectric material separates the two plates of capacitor.
b			(b) Water is pumped into one chamber. The membrane is stretched. Equal amount of water is forced out from the opposite chamber. On pumping more and more water, the pressure rises.	Battery connected across the capacitor forces positive charge on one plate and equal amount of negative charge on opposite plate. The capacitor is charged. The capacitor voltage continuously rises towards the battery voltage.
c			(c) When pressure developed by pump exactly equals tensile force of the membrane, the flow of water stops and pressure stabilises. The water cannot continuously flow only in one direction.	On reaching the battery voltage, the rise in capacitor voltage stops and current flow is zero, The voltage on capacitor stabilises at the battery voltage. Continuous DC current cannot flow through the capacitor.
d			(d) If pump stops running, the stretched membrane forces water flow in opposite direction The water coming out gives up energy.	If battery is removed and a resistance is connected across the capacitor, the capacitor forces a current in the opposite direction. The discharging current gives up stored electrical energy.
e			(e) If water is forced into the two chambers alternately, the membrane moves to and fro. Water flows in opposite direction alternately.	By applying an AC voltage across the capacitor, it continuously charges and discharges. The current flows in opposite directions alternately.
f			(f) If pump develops more pressure than that which the membrane can withstand, the membrane breaks and both chambers ae connected internally.	If a battery with a voltage much more than the rated voltage of the capacitor is connected, the capacitor breaks down, short circuiting both the plates internally.

op-amp frequency compensation... the why and the how

When an operational amplifier is used in a negative feedback circuit its frequency response requires 'compensation', a high-frequency rolloff that may be 'internal' or 'external'. With inadequate compensation the circuit will usually misbehave or even oscillate. This article will explain the reasons for frequency compensation, describe the usual 'simple' approach and then show how an 'external' type can be fitted with an improved compensation-arrangement. The latter approach results in a circuit that responds far better to large and fast excursions of the input signal.

Why does an operational amplifier need compensation? The story starts with the observation that parasitic capacitances in the IC itself cause the 'open-loop' (i.e. without-feedback) response of the device to roll off more or less sharply above a certain high frequency. This is illustrated by the drawn line in figure 1 – the 'uncompensated' response. The actual curve is bounded by asymptotes, 6 dB/octave (20 dB/decade) above f_1, 12 dB/octave above the second turnover point f_2 and even 18 dB/octave above f_3 in cases where there is a third turnover. The open-loop gain is constant from DC to f_1 (the real curve 3 dB 'down' at f_1), equal to the value A_{OL}. Figure 1 also shows the desired gain-with-feedback-operating, A_{cl} (in decibels). If the slope of the open-loop response at the intersection with the horizontal through A_{cl} exceeds 12 dB/octave, the actual feedback will start to become positive, as the total phase-shift will have exceeded 180°. With the values assumed in the figure the op-amp would certainly be in business for itself! The only way to 'dump' enough open loop gain before the phase-shift in the IC exceeds 180° is to provide HF rolloff, starting early enough – so that the intersection between the open-loop and closed-loop response curves occurs at 6 dB/octave. A step-network that 'flattens' again at f_1 (drawn curve in figure 2) is the standard trick. It will result in the dashed curve of figure 1.

The situation is in fact that the 'loop gain' falls below the amount that would enable oscillation, if the feedback were to become positive, at a point where there is still 90° phase-margin.

Note that many integrated op-amps have their frequency compensation built-in. An internal capacitor then displaces one of the 'stray' rolloffs so far downward in frequency that it dominates in the response, automatically providing the figure 1 dashed curve. Perhaps the best known example of this is the '741'.

Those op-amps that are intended for use with external compensation are supplied with data on how this should be done, given the required values of closed-loop gain, phase-margin etc. For most applications the instructions err on the 'safe' side.

That concludes the review of the basics of frequency-compensation. It is now time to take a closer look – preferably inside the IC! It will be convenient to assume the usual op-amp circuit of differential input stage, second stage with gain and some form of wideband unity-gain output stage (usually with local feedback and biassed in class B). The rolloff time-constant is normally inserted between the first and second stages or as a 'Miller' integration network in the second stage itself.

It is not difficult to see that an op-amp with the figure 1 dashed response, obtained by a 'slow' second stage, will have its input stage driven progressively harder above f_1, due to the failing feedback (6 dB/octave above f_1, 12 dB/octave above f_2).

There is a distinct danger that rapidly-changing high-amplitude signals will cause the input stage to momentarily saturate, at the steepest part of the waveform – usually the zero-crossing. This results in bursts of gross distortion – in audio amplifiers – known as Transient Intermodulation

The solution to this problem is to insert the compensation network at the amplifier input. Figure 3a shows how this is done for a non-inverting amplifier and figure 3b gives the inverting circuit. The figure also gives rules for determining the resistor and capacitor values required. Some op-amps will misbehave with nothing connected to their 'compensation' pins; it is not always immediately apparent why – so that no general rule can be given. A trick that usually works is to insert a series RC-pair that reduces the open-loop gain by 6 dB or so, in a step, at some frequency above the highest input but well below f_1, at the usual compensation position.

The insertion of the compensation ahead of the input stage removes the cause of slew-rate limiting and TIM; the drive level of the input stage proper no longer rises with frequency during the sloping part of the open-loop response.

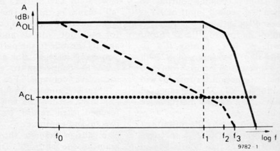
There is however a price to be paid, quite apart from the extra mess around the input pins. Noise from the input stage is no longer attenuated by the compensation network – it receives the full open-loop gain up to f_1. The kind of circuit in which TIM is a problem (high level) is however not usually so critical in respect of noise. Furthermore, the low source impedance at higher frequencies 'seen' by the input stage will tend to reduce its noise level anyway. ◼

Figure 1. The drawn line shows the op-amp's frequency response without 'compensation'. The dashed line shows the compensated or rolled-off response. At its point of intersection with the horizontal dotted line through A_{cl} (the so-called 'closed-loop gain', i.e. the amplication obtained with feedback operating), this response curve slopes at 6 dB/octave (20 dB/decade) – and the system is unconditionally stable.

Figure 2. A so-called 'step-network' compensation will cause the drawn line in figure 1 to follow the 'compensated' response curve shown dashed in figure 1.

Figure 3. Basic circuit and 'design rules' for improved compensation of a non-inverting (a) and an inverting amplifier (b).

1



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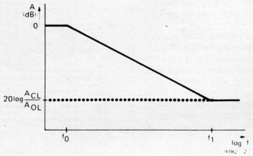

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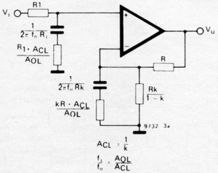

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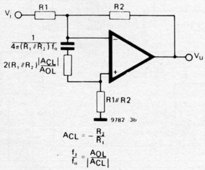


morse call sign generator

A.J.B.M. Peters

This new design offers the same facilities with considerably simpler circuitry, though at the expense of a slightly more complicated programming procedure.

It may be remembered that the previous design for a callsign generator used CMOS shift registers whose outputs were connected via diodes to two programming lines. This made for very simple programming but made the circuit fairly complicated. The programming of the new design is accomplished by storing the callsign in a 100 bit read only memory consisting of a diode matrix. A dot is stored in the matrix by inserting one diode in the required position. A dash, which has a duration equal to three dots, requires three diodes. A space within a character is of one dot duration and occupies one blank space (no diode) in the matrix. A space between letters is the same duration as a dash and thus occupies three blank spaces in the matrix. To generate the callsign the contents of the matrix are read out row by row.

100 bits may seem excessive, but it is possible for a single figure (digit ϕ) to occupy 19 spaces in the matrix. This, combined with long European call signs, soon uses up the spaces in the memory. British callsigns of 4 or 5 characters will, of course, not use as much of the memory capacity.

The complete circuit of the callsign generator is given in figure 1. The diode matrix is in the top left corner of the diagram. Readout is accomplished by addressing the rows and columns of the matrix using two 7490 decade counters and 7442 decoders.

The rate at which the callsign is repeated is determined by IC5, a 555 timer connected as a monostable multivibrator. Assume that initially the monostable is in the triggered condition. The output, pin 3, is high, so both the counters IC3 and IC4 are held in the reset condition. Output 0 of IC1 (column 0) and output 0 of IC2 (row a) are thus both low and all other outputs are high. One input of NOR gate N1 is low and the other is high, since no diode is connected in position 'a0' in the matrix as this is the rest position. The output of N1 is thus low. When the monostable (IC5) resets, the reset inputs of IC3 and IC4 go low and IC3 begins to count pulses from the clock generator built around S2. As the counter counts the column outputs 0 to 9 of IC1 go low in turn. Whenever a position is reached where a diode is connected from a column output to row 'a' then the second input of N1 is pulled low and the output goes high.

At the end of the first row the D output of IC3 will go low, causing IC4 to advance one step. One input of N2 will now be low and as IC3 counts from 0 to 9 again the information on row 'b' will be read out via N2. This is repeated until all the rows of the matrix have been read out.

The diodes connected to the outputs of N1 to N10 form an OR gate to route the information to the inputs of an audio tone generator S1 and a relay driver T1. When a dot or dash is present the tone generator is activated and the relay is energised. During spaces between character elements there is no tone and the relay drops out. The tone generator may be used to modulate a transmitter or the relay may be used for CW keying.

When a count of 100 has been reached all the rows of the matrix will have been read out. The D output of IC4 goes low on count 100. This negative-going edge is differentiated by the 1 n capacitor and 10 k resistor to produce a short pulse which triggers the 555, inhibiting the counters until the 555 resets again. The repetition rate of the callsign can be varied by means of P1.

Programming requires a fair number of diodes, the exact quantity depending on the actual callsign.

To programme the generator, start with row 'a' of the matrix. Leave position 'a0' blank as this is the rest position. Work along row 'a' and connect a diode for each dot with its anode to row 'a' and its cathode to the particular column you have reached. For a dash a diode must be connected to each of three successive columns. For a space the appropriate number of columns must be left blank. When the end of row 'a' is reached then return to the start of row 'b' and continue.

The callsign example shown in the diagram is the author's, DE PAϕARR, which in morse is

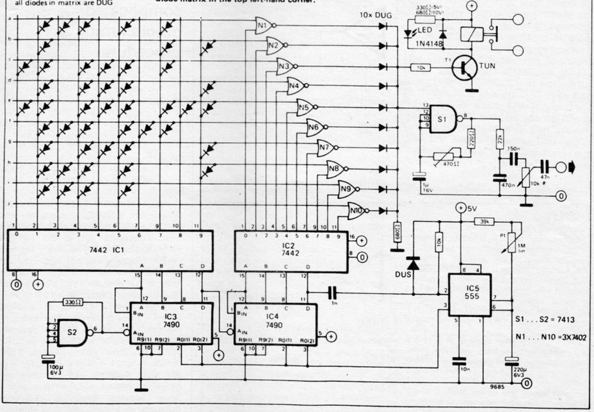
–. . . . – – . . – – – – – – . –
. – . . – .

This is laid out in the matrix as follows:

column

row	0	1	2	3	4	5	6	7	8	9
a		●	●	●		●		●		
b		●						●		●
c	●	●		●	●	●		●		
d		●		●	●	●				●
e	●	●		●	●	●		●	●	●
f		●	●	●		●	●	●		
g		●		●	●	●				●
h		●	●	●		●				●
i		●	●	●		●				
j										

Figure 1. Complete circuit of the callsign generator. The desired callsign is stored in the diode matrix in the top left-hand corner.



ELECTRONIC PIEZO-BUZZER IPB30

IPB30 is an economical version of ION's piezo-ceramic buzzer IPB35. This new model has only two wires, for direct connection to the supply.

Piezo-buzzers are based on a vibrator consisting of a thin disc of piezo-electric material and a metal disc. These electronic buzzes are a better replacement to the conventional electromagnetic buzzer, by virtue of their low power consumption. Non-switching characteristic of ION buzzers, avoids generation of electrical noise in the circuit. Sound is produced by direct application of DC voltage. There is no need of external components like transistors, capacitors, coils for oscillation or amplification.

This product finds applications in:

Household Appliances : Microwave oven, washing machine, Burglar/Firealarm, TV games, Alarm clocks, Toys.

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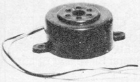

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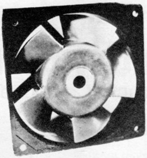
COOLING FAN

Hind Electric and Electronics have introduced a tube axial Fan model TAF-B-110-SSB. The fan is 121mm square by 39mm deep with an operating voltage 230V AC, 50 HZ, and power consumption 18 Watts. The housing is all metal and the motor is of shaded pole type with two single shield ball bearings mounted with extra lubricant reservior. The five bladed impeller is made out of polycarbonate for strength and light weight.



For Further details please contact

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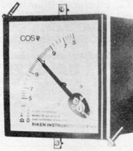

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Chandigarh - 1600 002.

PH METER KIT

ELECTRONICS India offers a portable "pH METER KIT". This Digital pH meter, combination electrode, buffer tablets, solution and buffer containers for laboratory and field use are all supplied in a Briefcase. The unit with liquid crystal display operates on a compact 9 Volts dry battery. It has automatic low battery indication on the display. Provision for optional external power pack is also given. Its resolution is 0.01 pH and impedence greater than 10^{11} ohms.

The products is suited for hospitals, chemical and pharmaceutical labs, research laboratories, and different industries.

For further information please contact:

M/s. Electronics India,
A-11/5, Vasant Vihar,
New Delhi - 110 057.

DE-SOLDERING PUMP

Marvel Industries have introduced a desoldering device for sucking molten solder instantly from PCBs. The nozzle is of Teflon to withstand high temperature. All spare parts are available.

For further information,
Marvel Industries,
208, Allied Industrial Estate,
Mahim, Bombay - 400 016.

TEMPERATURE CONTROLLER

Radix offers a linearised digital temperature controller type LTC 2000. This instrument accepts B,E,J,K,R,S or T thermocouple and 2/3 wire Pt100 sensor as also current/voltage inputs. Ranges cover 0 to 1820°C. The input characteristic is linearised by an 8085 based microcomputer using a look-up table. The linearisation accuracy is + 1°C. Overall indication accuracy is typically ±2°C at 30°C ambient. ON/OFF as well as time proportionating control are available. The output relay is an industry standard plug-in OEN make 67 series relay rated at 3A/110V. AC. LTC 2000 features automatic cold-junction compensation. It is failsafe for sensor break, with the relay switching off and the display flashing 'OPEN'. A 'WATCHDOG' timer guarantees secure operation in the noisiest industrial environments. The instrument is housed in a DIN standard 96(H) x 96(W) x 260(D) mm panel mounting case. Operating ambient is 5 to 45°C.

For further details write to:
M/s. Radix Electrosystems
A/22, Bonanza Ind. Estate
Kandivili (E), Bombay - 400 101.
Phone:: 699589

SMPS

M/s. Nartronics has developed Switch Mode Power Supply for colour T.V's. Available in two basic versions viz. Normal range: for input voltage 160V-290V A.C. and Wide range: 90V-290V A.C. Mains isolated it features over voltage overload and short circuit protection along with line load regulation, EMI and RFI suppression.

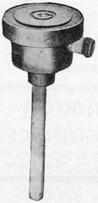
For further details, contact:

M/S NARTRONICS
A-36 Ultra co-op soc.
Dilip Gupte Road
Shivaji Park
Bombay-400 016 Phone: 455187

THERMO COUPLES

Chowdhury offers thermo couples for various applications in range -2006°C to +1600°C. Available in different lengths, the thermocouples have chromium plated Aluminium die cast connecting heads.

Special purpose thermocouples such as, for salt bath, molten metals, lock type (for P.V.C./Rubber etc.), pin type, disc type, bow type are also available.

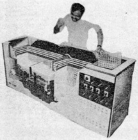


For Details, please write to:
M/S CHOWDHURY INSTRUMENTS PVT. LTD.
110, Model Basti,
New Delhi-110 005.

ULTRASONIC CLEANERS

Thorough clean Ultrasonics have introduced a range of ultrasonic cleaners to be used by electronic equipment manufacturers, mechanical part fabricators, electroplaters.

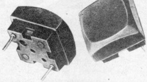
PCBs, electronic perts and compoents canbe freed from flux, fine metal dust, light oil etc. Connectors and press parts can be cleaned to remove grinding dusts, metallic powders, oil so that better and durable electroplating can be done.



For further details please contact:
M/S THROUGCLEAN ULTRASONICS,
5, Shiram Shimpoli road,
Borivili (W)
Bombay - 400 092.

KEYBOARD SWITCH

M/s. Darshana Industries has introduced a low profile Keyboard Switch. It is a 15mm x 15mm., Two terminal S.P.S.T. N/O Switch rates at 50M.A. 12 V. DC., and has a 1.0 mm movement. The terminals are 0.9 mm Tinned Copper Wire on a 10mm grid. It features a detachable A.B.S. keytop. Legends may be hot stamped or engraved onto the A.B.S. Top.



For Further details contact:
M/s. Darshana Industries
63, Industrial Estate, Hadapsar,
Pune - 411 013.
Phone: C/o 70253

LACING CORD

Novoflex lacing cord is made of soft & elastic PVC which when stretched for tying grips the cable bundle firmly. The resulting tie looks very neat and the knots are very fine.

Novofled Lacing Cord is entirely made of a very soft grade PVC micro crystal wax compound. It is highly resistant to chemicals and weather agents and is self extinguishing. It can withstand at temperature extreme of 90°C. Samples and specifications are forwarded on request.

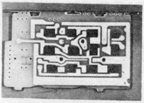
For further details, contact:
M/S NOVOFLEX CABLE INDUSTRIES
Block A-14, 7th Floor
Chatterjee International Centre
33 A, Chowringhee Road,
Calcutta-700 071

Phone: 29 04 82, 29 59 39, 29 39 91

THICK-FILM MATERIALS

Eletecks have developed a Thick-film Polymer Resistor (Series No:1100) for screen printing Resistors onto Phenolic boards, and Polyster Films. They are cured at 120°C for 1-2 hrs, and are available in the Sheet Resistivity Range from 1 Ohm/sq. to 10M Ohm/sq. with a tolerance of ± 30%. Thickness of the resistor film is about 15 mm using a 150 mesh Nylon screen.

Eletecks Thick-Film Polymer Resistor Series 1100 and the Eltecks Screen Printable Silver Conductor 1238-B, are useful in the manufacture of a variety of Electronic Circuits/Devices/Components such as : Membrane Key-boards, Push Button Telephones, Electrical Games & Toys, Presets & Potentiometers, Colour TV-Remote Control Switches, Light-sensitive Resistors, Circuits for Intercom, and for precision Electronic Instruments, etc.



For further details, please contact :
A. Sreenath
Marketing Executive
Eltecks Corporation C-314,
Industrial Estate, Peenya
Bangalore - 560 058.
Telephone No. 384002.
Telex: No. 0845-8328 KSIC IN
Attn: ELTECKS

DPM

This Digital Panel Meter is offered to OEMs. The manufacturer claims that this meter has basic accuracy of better than + 0.1% of the reading. It requires 5V DC to

operate with a basic range of 200mv or 2 V DC. The panel cutout size is 30 x 70mm.

For more details write to:
M/s. Jivan Electro Instruments.
394 G.I.D.C. Makarpura,
Baroda 390 010.

TEMPERATURE INDICATOR

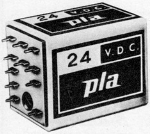
Radix offers a linearised digital temperature indicator type LTI 2000. This instrument accepts B,E,J, K,R, S or T thermocouple and 2/3 wire Pt100 sensor as also current/voltage inputs. Ranges cover -210 to 1820°C. The input characteristic is amplifed by a low-drift amplifier and linearised by an 8085 based microcomputer using a look-up table. The linearisation accuracy is ±1°C. Overall indication accuracy is typicall +20°C at 30°C ambient. LTI 2000 features automatic cold-junction compensation. In case of sensor break, the display flashes 'OPEN'. A 'WATCHDOG' timer guarantee secure operation in the noisiest industrial environment. The instrument is housed in a DIN standard 96(H) x 96(W) x 260(D) mm panel mounting case. Operating ambient is 5 to 45°C.

For further information write to:
Radix Electrosystems
A/22, Bonanza Ind. Estate,
Kandivili (E), Bombay - 400 101.
Phone: 699589

PCB RELAYS

PLA has introduced PCB relays which are similar to their series M Relays. These are available with 3 changeover and 2 changeover contacts with standard coil voltage of 12V and 24V DC. Relays of other coil voltage can also bé made available against bulk requirements.

Contacts are rated for 6 amps. resistive load at 250V AC/24V DC.



For further information please write to :

M/S SAI ELECTRONICS,
(A div. of Starch & Allied Industries)
Thakor Estate,
Kurla Kirol Road,
Vidyavihar (West)
Bombay - 400 086.

Phone : 5131219/5136601

LCD DPM

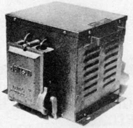
Elinco introducing 4½ digit LCD DPM offering low current consumption and compact size. The DPM 60 features Auto-zero, Auto-polarity, a logic switched 200m V or 2V fsd, Digital Hold, programmable decimal points and a 1mA current consumption. Automatic low battery indication and 'continuity' flags are built into the 10mm 4½ digit display. The DPM 60 can be readily scaled by user to indicate many different units, amps, volts, ohms etc. Supplied complete with fixing bezel, clips and connector, the DPM 60 will suit many applications calling for low-cost, high accuracy measurements in portable instruments.

For further information please contact:

M/S ELECTRONICS INDIA CO.
3749 Hill Road, Ambala Cantt-133 001
Phone: 0171-21770.
Cable: DIGITALS

AUTO TRANSFORMER

'MAHAVIR' Auto Transformers are available in Step-up, Step-down, single phase and three phase types ranging from 100 VA to 200 KVA capacity. These transformers are also made to individual requirements. Accessories like Tap-change Switch, On-Off Switch, Safety Fuse, Indication lamp, Voltmeter, Ameter etc. are can be also provided alongwith transformers.



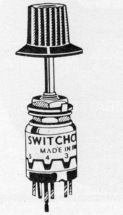
For further details please contact:

M/S SHEPHERD TRANSFORMERS,
Nityanand Nagar, Off Link Bridge, Ghatkopar (West), Bombay
Bombay - 400 086.

Phone: Office : 513 66 35
Works: 58 53 07

MINI SWITCH

SWITCHCRAFT offer subminiature rotary switches that are rated for 2-A-125V AC, and are available in 3 configurations, i) Single Pole-8 Position, ii) Double Pole-4 Position and iii) Four Pole-2 Position. These switches have an adjustable stop from 2 to 8 positions, switch base is transfer moulded with moulded-in terminals to prevent solder flux contamination. All contacts are made of silver and terminals are copper, silver plated. The switch is totally enclosed and the indexing mechanism is fully lubricated for life. The overall dimensions of the switch behind the panel are, 14.5 mm dia. x 28 mm length. The switches are supplied with rotary knob and mounting hardware.



For more information, write to:

M/S SWITCHCRAFT
24 Pankaj
Vakola Bridge,
Santacruz (E)
Bombay-400 055.

SWITCH MODE POWER SUPPLIES

Steadfast Electronics have developed switch mode Power supplies. These SMPS operate on 230V but can withstand a voltage variation from 180V to 264V. The output D.C. voltage remains constant within a close tolerance limit.

On account of their very high efficiencies, low heat disipation and use of components like ferrite cores, toroidalcores, ICs etc. these SMPS find increasing use as pwer supplies in TVs Computers, telecommunication equipment etc.

For further details, contact.

STEAD'FAST

STEAD'FAST ELECTRONICS CO.
Mill Stores House,
73, Tamarind Street,
BOMBAY-400 023.

INSTRUMENT TROLLEY

Elma Industries offers TROLLEY that is suitable for all types of Electronics Measuring Instruments. The stands are made of square pipe highly chrome plated. The shelves are made of 18 gauge M.S. Steel and finished in oven baked enamel paint. The Total height of the trolley is 32" from floor. Topshelf size 17½" Long X 11½" Wide. Middle shelf size 22" Long X 11½ wide. Distance between the top and middle shelf is 15". Distance between the middle & bottom shelf is 7" below the drawer. They also undertake special orders.

For further information, Please Contact :

ELMA INDUSTRIES
A/15, Aaram Society, Vakola Santacruz (East),
Bombay 400 055.
Telephone : 612 93 15.

classified ads

CORRECTIONS

In car ionizer

March 1987

The value of P 1 is given as 47 K in the parts list; its correct value is 10 K as shown in figure 1

advertisers index

elektor electronics

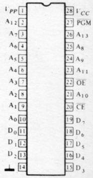
IMPORTANT

RE : DATA/INFO CARDS

- *Only data cards no. 28 & 29 have been published in our january 1987 issue.*
- *Our february 1987 issue, contains no cards whatsoever.*
- *From the March 1987 issue, the Data/Info cards are replaced by Data/Info sheets without disturbing the sequence.*

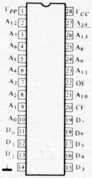
Elektor Electronics Info Sheet-123	Microcomputer-ICs 13	EPROMs Pin-outs

27128
HN4827128G-25



128 kilobit =
16K x 8 bit =
16384 byte

27256
HN4827C 256G-25



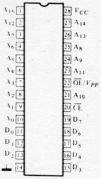
256 kilobit =
32K x 8 bit =
32768 byte

Elektor Electronics Data Sheet-30	Transistors BD241 & BD242

Type	Characteristics		Limits	
The BD241 is an n-p-n transistor intended for power amplifiers and fast switching applications	Collector cut-off current, $\lvert I_{CEO} \rvert$ BD241; BD241A; BD242; BD242A ($\lvert U_{CE} \rvert$ = 30 V) BD241B; BD241C; BD242B; BD242C ($\lvert U_{CE} \rvert$ = 60 V) BD241D; BD241E; BD241F; BD242D; BD242E; BD242F ($\lvert U_{CE} \rvert$ = 90 V)	≤300 μA	$\lvert U_{CEO} \rvert$	see reverse side
	Emitter cut-off current, I_{EBO} ($\lvert U_{BE} \rvert$ = 5 V; $\lvert I_C \rvert$ = 0 mA)	≤1 mA	$\lvert U_{CER} \rvert$	see reverse side
	Base-emitter on voltage, U_{BE} ($\lvert U_{CE} \rvert$ = 4 V; $\lvert I_C \rvert$ = 3 A)	≤1.8 V	$\lvert U_{EBO} \rvert$	5 V
The BD242 is a p-n-p transistor intended for power amplifiers and fast switching applications	Collector-emitter saturation voltage, $\lvert U_{CE(sat)} \rvert$ (BD241,BD241A,BD241B,BD241C;BD242;BD242A; BD242B;BD242C: $\lvert I_B \rvert$ = 0.6 A; $\lvert I_C \rvert$ = 3 A)	≤1.2 V	$\lvert I_{CAV} \rvert$	3 A
	(BD241D;BD241E;BD241F;BD242D;BD242E;BD242F: $\lvert I_B \rvert$ = 0.75 A; $\lvert I_C \rvert$ = 3 A)	≤2.5 V	$\lvert I_{CM} \rvert$	5 A
	DC current gain, h_{FE} (all types: $\lvert U_{CE} \rvert$ = 4 V; $\lvert I_C \rvert$ = 1 A)	≥25	$\lvert I_B \rvert$	1 A
	(BD241;BD241A;BD241B;BD241C;BD242;BD242A; BD242B;BD242C: $\lvert U_{CE} \rvert$ = 4 V; $\lvert I_C \rvert$ = 3 A)	≥10	P_D	40 W*
	(BD241D;BD241E;BD241F;BD242D;BD242E;BD242F: $\lvert U_{CE} \rvert$ = 4 V; $\lvert I_C \rvert$ = 3 A)	≥5	T_j	150 °C
	Data are valid only for conditions stated.		*up to = 25°C; without heat sink 2 W at T_C = 25°C	

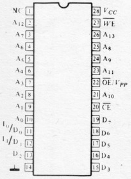
Elektor Electronics **Info Sheet-123**	Microcomputer ICs 13	EPROMs Pin-outs

27512



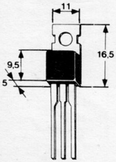
512 kilobit =
64K x 8 bit =
65536 byte

27513



4 pages each with
16K x 8 bit
I_0 - I_1 page select
D_1 - D_7 data

Elektor Electronics **Data Sheet-30**	Transistors BD241 & BD242



B C E
TO–220 AB

Dimensions in mm

The various types in these series differ in collector-emitter voltages:

	$\lvert U_{CEO}\rvert$*	$\lvert U_{CER}\rvert$**	
BD241; BD242	45	55	V
BD241A; BD242A	60	70	V
BD241B; BD242B	80	90	V
BD241C; BD242C	100	115	V
BD241D; BD242D	120	160	V
BD241E; BD242E	140	180	V
BD241F; BD242F	160	200	V

* at $\lvert I_C\rvert$ = 30 mA
**with R_{BE} = 100 R

Transistor BD241 is complementary to the Type BD242.

The collector of these transistors is connected to the metal case.

Thermal resistance, R_{th}
junction to case, $R_{th(j\text{-}c)}$ max 3.125 K/W
junction to ambient, $R_{th(j\text{-}a)}$ max 62.5 K/W

The BD241 is the European equivalent of the TIP31
The BD242 is the European equivalent of the TIP32

MH/BY WEST - 228
LIC No 91

Printer & Publisher — C.R. Chandarana, 2, Koumari, 14th A Road, Khar, Bombay 400 052.
Printed at Trupti Offset, 103 Vasan Udyog Bhavan, Tulsi Pipe Road, Lower Parel, Bombay 400 013.